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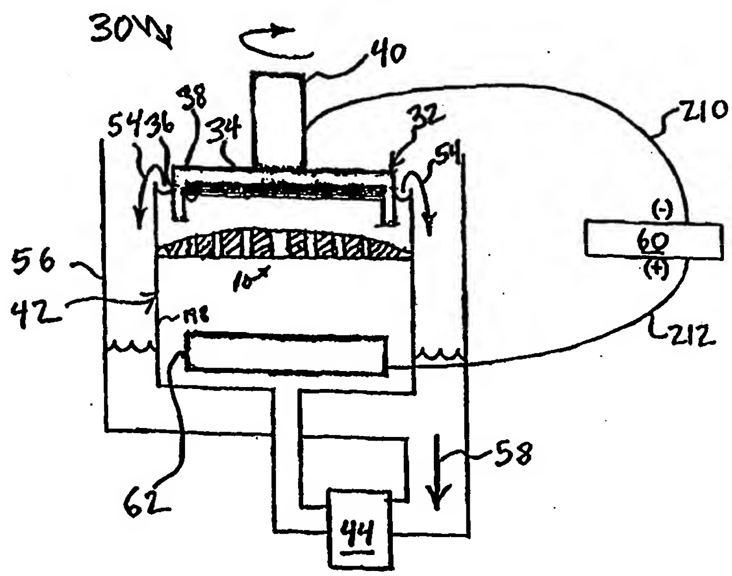

(57) Abstract

An apparatus (30) for depositing an electrical conductive layer on the surface of a wafer (38) includes a virtual anode (10) located between the actual anode (62) and the wafer (38). The virtual anode (10) modifies the electric current flux and plating solution flow between the actual anode (62) and the wafer (38) to thereby modify the thickness profile of the deposited electrically conductive layer on the wafer (38). The virtual anode (10) can have openings through which the electrical current flux passes. By selectively varying the radius, length or both, of the openings, any desired thickness profile of the deposited electrically conductive layer on the wafer (38) can be readily obtained.

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VIRTUAL ANODE DESIGN FOR USE IN WAFER PLATING

CROSS REFERENCE TO RELATED APPLICATION

This application is related to Patton et al., co-filed Application Serial No. [Attorney Docket No. M-4269 US]; Contolini et al., co-filed Application Serial No. [Attorney Docket No. M-4898 US]; and Reid et al., co-filed Application Serial No. [Attorney Docket No. M-4272 US], all of which are incorporated herein by reference in their entirety.

FIELD OF INVENTION

The present invention relates generally to an apparatus for treating the surface of a substrate and more particularly to an apparatus for electroplating a layer on a semiconductor wafer.

BACKGROUND OF THE INVENTION

The manufacture of semiconductor devices often requires the formation of electrical conductors on semiconductor wafers. For example, electrically conductive leads on the wafer are often formed by electroplating (depositing) an electrically conductive layer such as copper on the wafer and into patterned trenches.

Electroplating involves making electrical contact with the wafer surface upon which the electrically conductive layer is to be deposited (hereinafter the "wafer plating surface"). Current is then passed through a plating solution (i.e. a solution containing ions of the element being deposited, for example a solution containing Cu^{++}) between an anode and the wafer plating surface (the wafer plating surface being the cathode). This causes an electrochemical reaction on the wafer plating surface which results in the deposition of the electrically conductive layer.

To minimize variations in characteristics of the devices formed on the wafer, it is important that the electrically conductive layer be deposited uniformly (have a uniform thickness) over the wafer plating surface. However, conventional electroplating processes produce nonuniformity in the deposited electrically conductive layer due to the "edge effect" described in Schuster et al., U.S. Patent No. 5,000,827, herein incorporated by reference in its entirely. The edge effect is the tendency of the deposited electrically conductive layer to be thicker near the wafer edge than at the wafer center.

To offset the edge effect, Schuster et al. teaches non-laminar flow of the plating solution in the region near the edge of the wafer, i.e., teaches adjusting the flow characteristics of the plating solution to reduce the thickness of the deposited electrically conductive layer near the wafer edge. However, the range over which the flow characteristics can be thus adjusted is limited and difficult to control. Therefore, it is desirable to have a method of offsetting the edge effect which does not rely on adjustment of the flow characteristics of the plating solution.

Another conventional method of offsetting the edge effect is to make use of "thieves" adjacent the wafer. By passing electrical current between the thieves and the anode during the electroplating process, electrically conductive material is deposited on the thieves which otherwise would have been deposited on the wafer plating surface near the wafer edge where the thieves are located. This improves the uniformity of the deposited electrically conductive layer on the wafer plating surface. However, since electrically conductive material is deposited on the thieves, the thieves must be removed periodically and cleaned, thus adding to the maintenance cost and downtime of the apparatus. Further, additional power supplies must be provided to power the thieves, adding to the capital cost of the apparatus. Accordingly, it is desirable to avoid the use of thieves.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a "virtual" anode between the actual anode (hereinafter "the anode") and the wafer plating surface. This virtual anode, made of an electrically insulating material, acts to modify the electric current flux and the plating solution flow between the anode and the wafer plating surface in a manner which can be controlled by the shape and location of this virtual anode. Since the thickness of the deposited electrically conductive layer at any particular region of the wafer plating surface is determined by the electric current flux to the particular region, this virtual anode permits any desired thickness profile of the deposited electrically conductive layer.

In one embodiment, the virtual anode takes the form of a member positioned between the anode and the wafer plating surface, this member having at least one opening therein through which plating solution flows. This virtual anode has the effect of regulating both the electric current flux and the plating solution flow between the anode and the wafer plating surface, depending upon the shape and location of the virtual anode. The virtual anode also has the effect of "decoupling" the electric current flux from the plating solution flow so that the two variables may be controlled independent of each other.

In one embodiment of the invention, the virtual anode has a plurality of opening therein, at least one of which is of a different cross-sectional area than at least one of the others, or is of a different length, or both. In general, a change in the cross-sectional area of an opening produces a greater change in the plating solution flow than in the electric current flux through the opening. Thus, by using openings of different cross-sectional area, the plating solution flow can be decoupled (independently varied) from the electric current flux through the openings. In contrast, a change in the length of an opening produces a linear change in both the plating solution flow and the electric current flux through the opening.

In one particular embodiment, the openings are cylindrical. In this embodiment, the electric current through any particular opening is inversely proportional to the length of the opening and is directly proportional to the square of the radius of the opening. The plating solution flow through any particular opening is also inversely proportional to the length of the opening. However, in contrast to the electric current flux which is directly proportional to the square of the radius of the opening, the plating solution flow through any particular opening is directly proportion to the cube of the radius of the opening. Similar relations exist for openings of other shapes. Thus, by combining various openings of variable length and variable cross-sectional area, electric current flux and plating solution flow to the wafer can be controlled and, if desired, decoupled from one another. This allows any desired thickness profile of the deposited electrically conductive layer on the wafer plating surface to be obtained.

In a first alternate embodiment, the virtual anode is in the form of an annulus attached to an anode cup of the anode. This virtual anode acts as a shield to limit the amount of electric current flux at the edge region of the wafer by forcing the electric current flux to pass around the virtual anode, thereby reducing the thickness of the deposited electrically conductive layer on the wafer edge region.

In the second alternative embodiment, intended for use when it is desired to have a relatively thick deposit on the edge region of the wafer and a relatively thin deposit on the center region, the virtual anode comprises a disk overlying the center of the anode. This virtual anode effectively shields the center region of the wafer from the electric current flux thereby reducing the thickness of the deposited electrically conductive layer on the center region.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a diagrammatic view of an electroplating apparatus having a virtual anode mounted therein in accordance with the present invention;

FIG. 2 is a cross-sectional view of an electroplating apparatus and one embodiment of a virtual anode in accordance with the present invention;

FIG. 3 is a diagrammatic representation of the effect of a virtual anode having variable length openings on the electric current flux between the anode and the wafer plating surface in accordance with the present invention;

FIG. 4 is a diagrammatic representation of the effect of a virtual anode having variable radius openings on the electric current flux between the anode and the wafer plating surface in accordance with the present invention;

FIG. 5 is a cross-sectional view of an alternate embodiment of the virtual anode in accordance with the present invention;

FIG. 6 is a cross-sectional view illustrating another embodiment of a virtual anode which acts to shield the edge region of the wafer in accordance with the present invention; and

FIG. 7 is an isometric view of a further embodiment of a virtual anode which acts to shield the center region of the wafer in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a diagrammatic view of an electroplating apparatus in accordance with the present invention. Apparatus 30 includes a clamshell 32 mounted on a rotatable spindle 40 which provides rotation of clamshell 32. Clamshell 32 comprises a cone 34 and a cup 36. A clamshell of a type for use as clamshell 32 is

described in detail in Patton et al., co-filed Application Serial No. [Attorney Docket No. M-4269], identified above.

During the electroplating process, a wafer 38 preferably having an electrically conductive seed layer thereon is mounted in cup 36. Clamshell 32 and hence wafer 38 are then placed in a plating bath 42 containing a plating solution. The plating solution is continually provided to plating bath 42 by a pump 44. Generally, the plating solution flows upwards through openings in anode 62 and around anode 62 (to be explained further in connection with FIG. 2) toward wafer 38.

Disposed between anode 62 and wafer 38 is one embodiment of a virtual anode 10 in accordance with this invention. The periphery of virtual anode 10 is secured to a cylindrical wall 198 of plating bath 42 and is positioned at a distance from wafer 38 which is determined by the desired thickness profile of the electrically conductive layer to be deposited on wafer 38. The general rule is that the closer virtual anode 10 is to wafer 38, the greater the influence virtual anode 10 has on the resulting thickness profile of the electrically conductive layer to be deposited on wafer 38, as will be described in more detail below. Since virtual anode 10 is secured (sealed) to wall section 198 of plating bath 42, the plating solution flows through virtual anode 10. After flowing through virtual anode 10, the plating solution then overflows plating bath 42 to an overflow reservoir 56, as indicated by arrows 54. The plating solution is filtered (not shown) and returned to pump 44 as indicated by arrow 58, completing the recirculation of the plating solution.

A DC power supply 60 has a negative output lead 210 electrically connected to wafer 38 through one or more slip rings, brushes and contacts (not shown). The positive output lead 212 of power supply 60 is electrically connected to anode 62 located in plating bath 42. During use, power supply 60 biases wafer 38 to have a negative potential relative to anode 62, causing an electrical current to

flow from anode 62 through virtual anode 10 to wafer 38. As used herein, electrical current flows in the same direction as the net positive ion flux and opposite the net electron flux, wherein electric current is defined as the amount of charge flowing through an area per unit time. This also causes an electric current flux from anode 62 through virtual anode 10 to wafer 38, wherein electric current flux is defined as the number of lines of forces (field lines) through an area. This causes an electrochemical reaction (e.g. $Cu^{++} + 2e^{-} = Cu$) on wafer 38 which results in the deposition of the electrically conductive layer (e.g. copper) on wafer 38. The ion concentration of the plating solution is replenished during the plating cycle by dissolving a metal in anode 62 which includes, for example, a metallic compound (e.g. $Cu = Cu^{++} + 2e^{-}$), as described in detail below.

FIG. 2 is a cross-sectional view of anode 62 and virtual anode 10 in plating bath 42, plating bath 42 including cylindrical wall section 198. Anode 62 comprises an anode cup 202, ion source material 206, and a membrane 208. Anode cup 202 is typically an electrically insulating material such a polyvinyl chloride (PVC). Anode cup 202 comprises a disk shaped base section 216 having a plurality of spaced opening 216A therein through which plating solution flows. Anode cup 202 further comprises a cylindrical wall section 218 integrally attached at one end (the bottom) to base section 216.

An electrical contact and filter sheet is typically provided, as shown in detail in the co-pending application Reid et al., Serial No. [Attorney Docket M-4272 US] identified above. The contact 204 may be in the form of an electrically conductive, relatively inert mesh such as titanium mesh, and rests on the filter sheet which rests on base section 216 of anode cup 202. Resting on and electrically connected with contact 204 is ion source material 206, for example copper. During use, ion source material 206 electrochemically dissolves (e.g. $Cu = Cu^{2+} + 2e^{-}$), replenishing the ion concentration of the plating solution.

Ion source material 206 is contained in an enclosure formed by anode cup 202 and membrane 208. More particularly, membrane 208 forms a seal at its outer circumference with a second end (the top) of wall section 218 of anode cup 202. Although allowing electrical current to flow through, membrane 208 has a high electrical resistance which produces a voltage drop across membrane 208 from the lower surface to the upper surface. This advantageously minimizes variations in the electric field from ion source material 206 as it dissolves and changes shapes.

In addition to having a porosity sufficient to allow electrical current to flow through, membrane 208 also has a porosity sufficient to allow plating solution to flow through membrane 208, i.e. has a porosity sufficient to allow liquid to pass through membrane 208. However, to prevent particulates generated by ion source material 206 from passing through membrane 208 and contaminating the wafer, the porosity of membrane 208 prevents large size particles from passing through membrane 208. Generally it is desirable to prevent particles greater in size than one micron (1.0 μm) from passing through membrane 208.

Virtual anode 10 extends between and is attached on its entire outer periphery to wall 198 of plating bath 42. In the embodiment illustrated in FIG. 2, virtual anode 10 has a curved cross-section, being thinnest at the edge (periphery) and increasing in thickness toward the center. Virtual anode 10 is provided with a plurality of openings 10a - 10i extending through virtual anode 10 from the bottom side (the side facing anode cup 202) to the upper side. Openings 10a - 10i each have a different length, opening 10e in the center of virtual anode 10 being the longest and openings 10d - 10a and openings 10f - 10i being of gradually reduced length as illustrated. Further, opening 10e in the center of virtual anode 10 has the largest radius, while openings 10c, 10d and openings 10f, 10g have a smaller radius, and openings 10a, 10b and openings 10h, 10i have an even smaller radius. In the embodiment of FIG. 2, openings 10d, 10c and openings 10f and 10g have equal radii, while openings 10b, 10a and openings 10h, 10i have radii which are smaller than the remainder of the openings but are equal to each other. However,

this is a matter of choice, the important point being that the openings control both the electric current flux and the plating solution flow through virtual anode 10.

Representative dimensions for a typical plating apparatus in accordance with FIG. 2 are given in Table 1.

Table 1

Characteristic	Dimension
X	8.0 In.
Y	9.0 In.
Z	10.0 In.
A	1.0 In.
B	1.0 In.
C	1.0 In.
D	1.5 In.
E	4.89 In.
F	7.05 In.

FIG. 3 diagrammatically illustrates one example of the action of cylindrical openings in a virtual anode in modifying the electric current flux and the plating solution flow through the virtual anode. An electric current flux represented by flux lines F is established between anode 62B and wafer 38, and this electric current flux is uniform in the immediate vicinity of anode 62B. However, the presence of virtual anode 100A between anode 62B and wafer 38 modifies both the electric current flux and the plating solution flow. The effect on the electric current flux of the length of the openings in the virtual anode may be likened to a variable resistance, the longer the path through the virtual anode, the greater the electrical "resistance" to the electric current flux. More particularly, the change in electric current flux through any particular opening is inversely proportional to the length of the opening. This is illustrated in FIG. 3 where openings 100b and 100c are longer than openings 100a and 100d and thus present more electrical resistance

than do openings 100a, 100d. Hence, more electric current flux (i.e. a greater percentage of the total electric current flux to wafer 38) and more flux lines F pass through the shorter openings 100a and 100d than pass through the longer openings 100b and 100c resulting in a greater thickness of the deposited electrically conductive layer on the wafer edge region. (A greater electric current flux to a particular wafer region results in a greater thickness of the deposited electrically conductive layer at that region.)

The plating solution flow through any particular opening is also inversely proportional to the length of the opening. Thus, although openings 100a-100d of FIG. 3 have equal radii, the greater length of openings 100b, 100c will reduce the plating solution flow therethrough compared to openings 100a and 100d.

For purposes of illustration, assume the case where openings 100b and 100c are twice the length of openings 100a and 100d. Accordingly, there will be twice the electric current flux and twice the plating solution flow through openings 100a and 100d compared to openings 100b and 100c. Thus, a change in the length of an opening causes a linear change in both the electric current flux and plating solution flow through the opening. Accordingly, a change in length of an opening does not decouple the electric current flux from the plating solution flow.

FIG. 4 diagrammatically illustrates another example of the action of cylindrical openings in a virtual anode in modifying the electric current flux and plating solution flow through the virtual anode and, more particularly, in decoupling the electric current flux from the plating solution flow. In FIG. 4, all openings 100e-100h have equal length, but openings 100e and 100h have a greater radius than openings 100f and 100g. The electric current flux through any particular opening is directly proportional to the square of the radius of the opening. However, the plating solution flow through any particular opening is directly proportional to the cube of the radius of the opening. Thus, plating solution flow will be significantly greater through openings 100e and 100h

compared to openings 100f and 100g. The electric current flux, represented by flux lines F, will also be greater through openings 100e and 100h compared to openings 100f and 100g, although to a lesser extent than plating solution flow. Thus, the percentage of the total plating solution flow to wafer 38 is significantly greater through openings 100e and 100h compared to the smaller radius openings 100f and 100g while the percentage of the total electric current flux to wafer 38 is only somewhat greater through openings 100e and 100h compared to the smaller radius openings 100f and 100g.

Since a change in the radius of an opening produces a non-linear change in the electric current flux compared to the plating solution flow through the opening, to decouple the electric current flux from the plating solution flow, the radii of the openings are adjusted. In one embodiment, by using a plurality of small radius openings in contrast to a lesser number of larger radius openings, the total cross-sectional areas of the small radius openings and the larger radius openings being the same, the plating solution flow is restricted while the electric current flux remains essentially unchanged through the openings.

FIG. 5 illustrates an alternate embodiment of a virtual anode involving a stepped cross-section rather than the contoured cross-section of the virtual anode of FIG. 2. Virtual anode 10A has a plurality of openings therein 10j-10r which are generally similar in configuration and location to openings 10a-10i in the embodiment of FIG. 2. The only difference between the two embodiments is that, for ease of fabrication, virtual anode 10A is of a stepped construction. The operation of the embodiment of FIG. 5 is similar to that described above for FIG. 2, with the variable lengths and variable radius of openings 10j-10r controlling the electric current flux and the plating solution flow through virtual anode 10A. The dimensions given in Table I for the embodiment of FIG. 2 generally apply to the embodiment of FIG. 5.

Although the embodiment of FIG. 2 and FIG. 5 both illustrate virtual anodes which restrict the plating solution flow to the wafer edge region compared

to the center region wnile providing a relatively uniform electric current flux to the wafer plating surface, it will be apparent that other embodiments of the invention are possible, including configurations which reduce the electric current flux and plating solution flow to the central region of the wafer compared to the edge region, as shown in FIG. 7.

FIG. 6 diagrammatically illustrates another alternate embodiment of the invention in which the virtual anode 250 takes the form of an annulus extending inwardly from the top of wall section 218 of anode cup 202. Virtual anode 250 is a suitable electrical insulating material and acts as a shield for the flux lines F emanating through membrane 208 reducing the thickness of the deposited electrically conductive layer on the edge region of wafer 38. Important dimensions are illustrated in FIG. 6 and include the distance D between virtual anode 250 and wafer 38, the distance R which virtual anode 250 extends inward from anode cup 202, and the distance S representing the spacing between virtual anode 250 and membrane 208. Generally, the greater distance R is, and the smaller distances D, S are, the greater the shielding of the wafer edge region by virtual anode 250. Since each of these dimensions affect the flux lines F reaching wafer 38 and hence the thickness profile of the deposited electrically conductive layer, the thickness profile can be readily adjusted to suit the particular application by adjusting these dimensions.

FIG. 7 illustrates a further embodiment of the invention which is adapted for use where it is desired to have less deposited on the center region of the wafer. In that situation, virtual anode 260 takes the form of a disk of a suitable insulating material which overlies the center of anode 62A. Virtual anode 260 is suspended by rib-like members 261 which may be attached to anode cup 202 and overlie membrane 208. Virtual anode 260 effectively blocks the electric current flux and plating solution flow to the center region of the wafer, thereby reducing the thickness of the deposited electrically conductive layer at the center region of the wafer. In an alternative embodiment (not shown), a jet or tube is passed through

the center of anode 62A and through the center of virtual anode 260 to direct plating solution at the center region of the wafer as further described in Reid et al., Application Serial No. [Attorney Docket No. M-4272 US], cited above.

Having thus described the preferred embodiments, persons skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention. Thus, the invention is limited only by the following claims.

WE CLAIM:

1. A apparatus for treating the surface of a substrate comprising:

a clamshell for holding said substrate;

a plating bath comprising a wall section;

a virtual anode having a periphery secured to said wall section, said virtual anode having at least one opening therein; and

an anode, said virtual anode being located between said clamshell and said anode.

2. The apparatus of Claim 1 wherein said virtual anode has a plurality of openings therein.

3. The apparatus of Claim 2 wherein at least one of said plurality of openings has a different length than at least one other of said plurality of openings.

4. The apparatus of Claim 2 wherein at least one of said plurality of openings has a different radius than at least one other of said plurality of openings.

5. The apparatus of Claim 2 wherein at least one of said plurality of openings has a different radius and a different length than at least one other of said plurality of openings.

6. The apparatus of Claim 1 wherein said virtual anode has a contoured cross-section.

7. The apparatus of Claim 1 wherein said virtual anode has a stepped cross-section.

8. The apparatus of Claim 1 further comprising a plating solution, wherein said plating solution flows in said plating bath from said anode to said clamshell through said at least one opening.

9. The apparatus of Claim 8 further comprising a power supply for generating an electric current flux between said surface of said substrate and said anode.

10. The apparatus of Claim 9 wherein said electric current flux passes through said virtual anode.

11. The apparatus of Claim 10 wherein said virtual anode has a plurality of openings therein, a first opening of said plurality of openings having a greater length than a second opening of said plurality of openings, said first opening having a greater electrical resistance to said electric current flux than said second opening.

12. The apparatus of Claim 11 wherein a greater percentage of said electric current flux passes through said second opening than through said first opening.

13. The apparatus of Claim 10 wherein said virtual anode has a plurality of openings therein, a first opening of said plurality of openings having a greater radius than a second opening of said plurality of openings, said second opening having a greater electrical resistance to said electric current flux than said first opening.

14. The apparatus of Claim 13 wherein a greater percentage of said electric current flux passes through said first opening than through said second opening.

15. The apparatus of Claim 1 wherein said virtual anode comprises an electrically insulating material.

16. A method of treating a surface of a substrate comprising the steps of:

providing a clamshell, an anode, a virtual anode and a plating bath containing a plating solution;

mounting said substrate in said clamshell;

placing said clamshell and said substrate in said plating solution; and

generating an electric current flux between said surface of said substrate and said anode, wherein said electric current flux passes through said virtual anode, said virtual anode shaping said electric current flux.

17. The method of Claim 16 wherein said virtual anode has a plurality of openings therein, wherein said electric current flux passes through said plurality of openings and thereby through said virtual anode.

18. The method of Claim 17 wherein a first opening of said plurality of openings has a greater length than a second opening of said plurality of openings, a greater percentage of said electric current flux passing through said second opening than through said first opening.

19. The method of Claim 18 wherein the electric current flux through said first opening and said second opening is inversely proportional to the length of said first opening and said second opening.

20. The method of Claim 18 further comprising the step of generating a flow of said plating solution through said virtual anode, wherein a greater percentage of said plating solution flow passes through said second opening than through said first opening.

21. The method of Claim 20 wherein the plating solution flow through said first opening and said second opening is inversely proportional to the length of said first opening and said second opening.

22. The method of Claim 20 wherein the difference in plating solution flow through said first opening and said second opening is linear to the difference in electric current flux through said first opening and said second opening.

23. The method of Claim 17 wherein a first opening of said plurality of openings has a greater cross-sectional area than a second opening of said plurality of openings, a greater percentage of said electric current flux passing through said first opening than through said second opening.

24. The method of Claim 23 wherein said first opening and said second opening are cylindrical, the electric current flux through said first opening and said second opening being directly proportional to the square of the radius of said first opening and said second opening.

25. The method of Claim 24 further comprising the step of generating a flow of said plating solution through said virtual anode, wherein a greater percentage of said plating solution flow passes through said first opening than through said second opening.

26. The method of Claim 25 wherein the plating solution flow through said first opening and said second opening is directly proportional to the cube of the radius of said first opening and said second opening.

27. The method of Claim 26 wherein the difference in plating solution flow through said first opening and said second opening is non-linear to the difference in electric current flux through said first opening and said second opening.

28. The method of Claim 27 wherein the difference in plating solution flow through said first opening and said second opening is greater than a difference in electric current flux through said first opening and said second opening.

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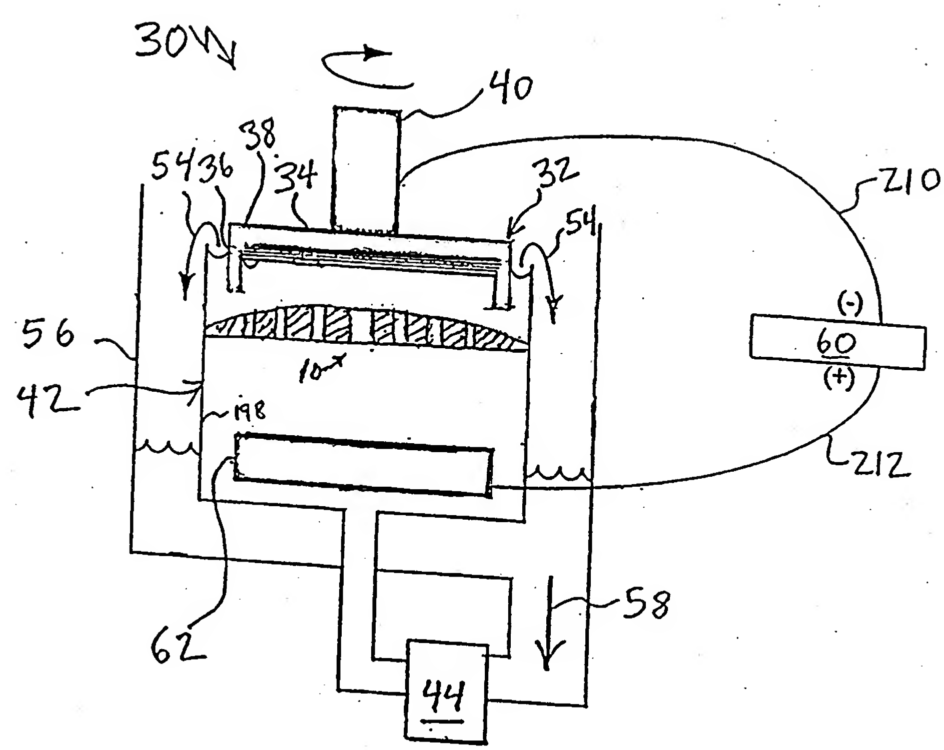

FIG. 1

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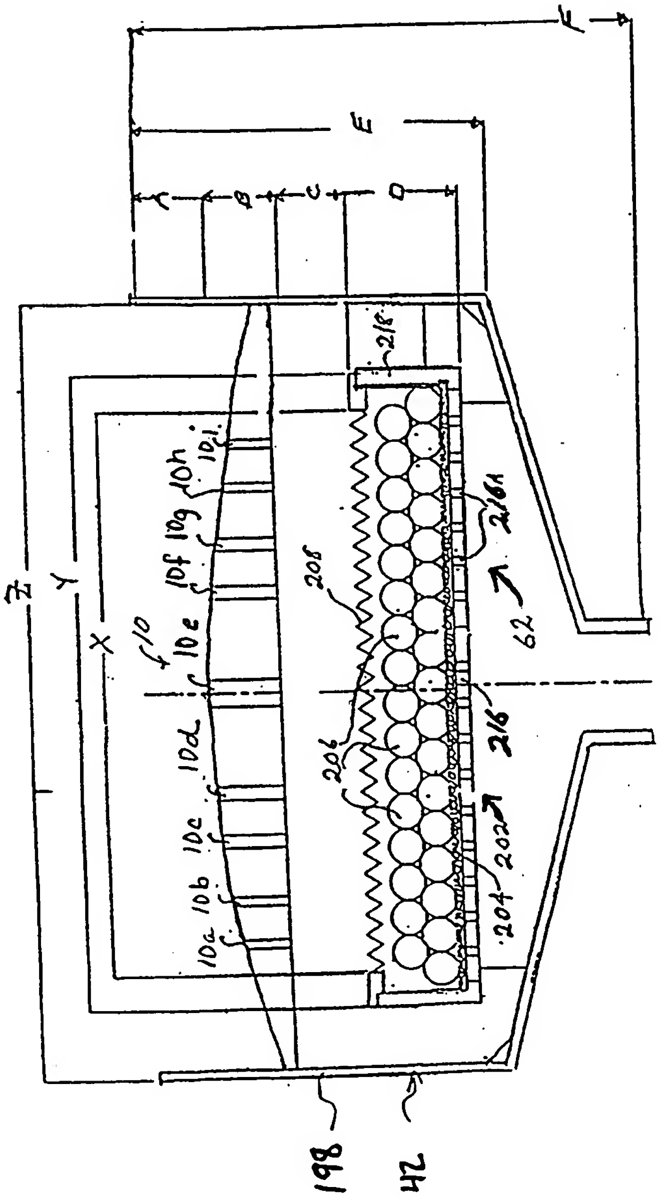

FIG 2

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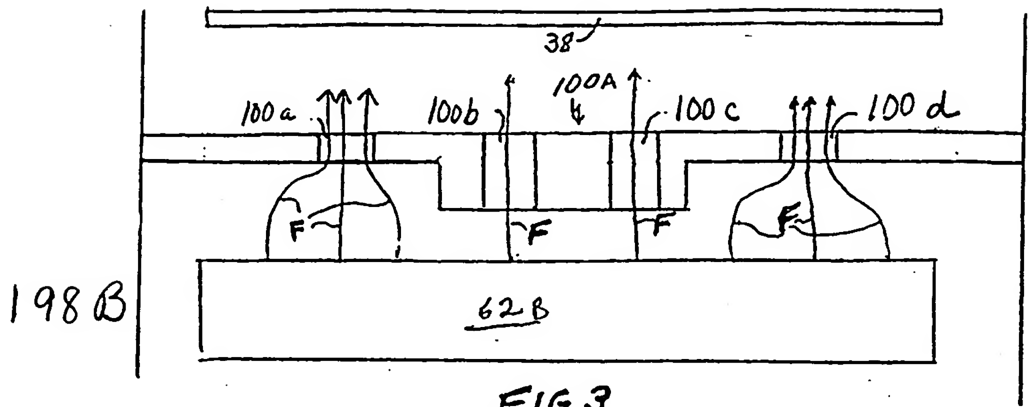

FIG 3

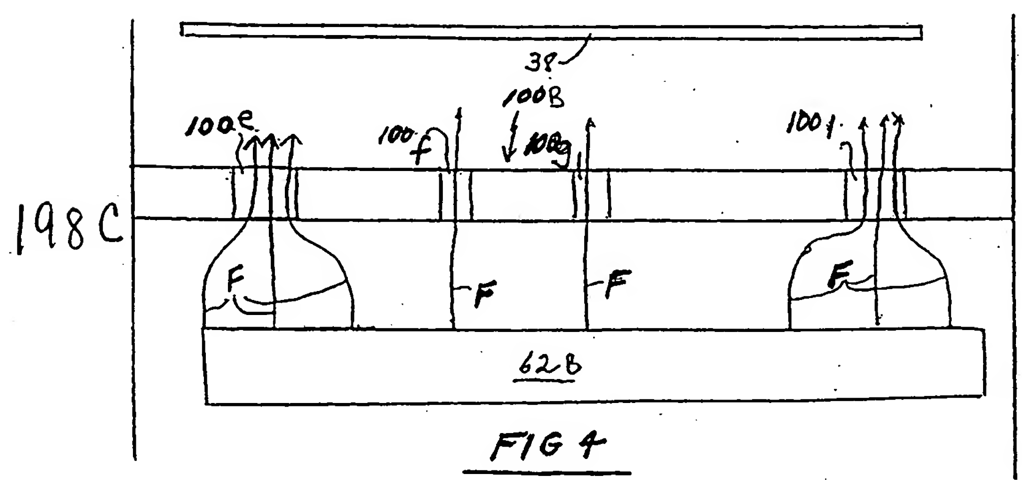

FIG 4

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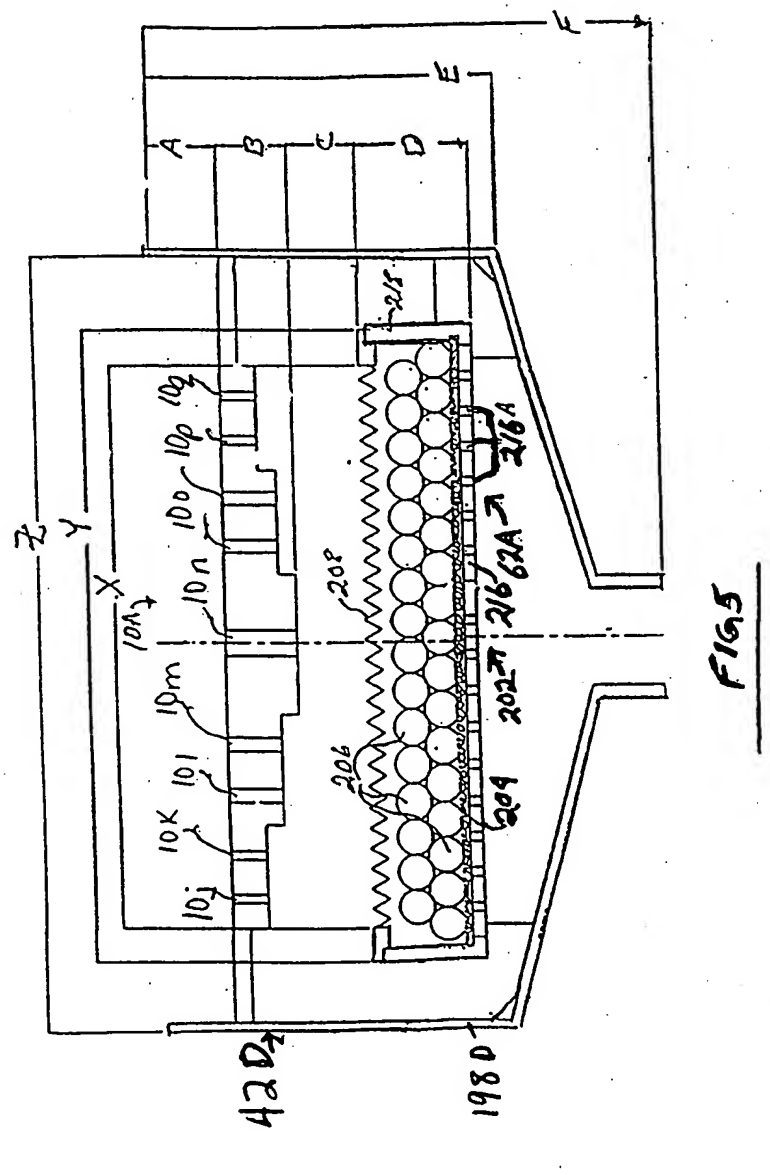
FIG 5
A
B
C
D
E
F
X
Y
Z
10j
10K
10l
10m
10n
10o
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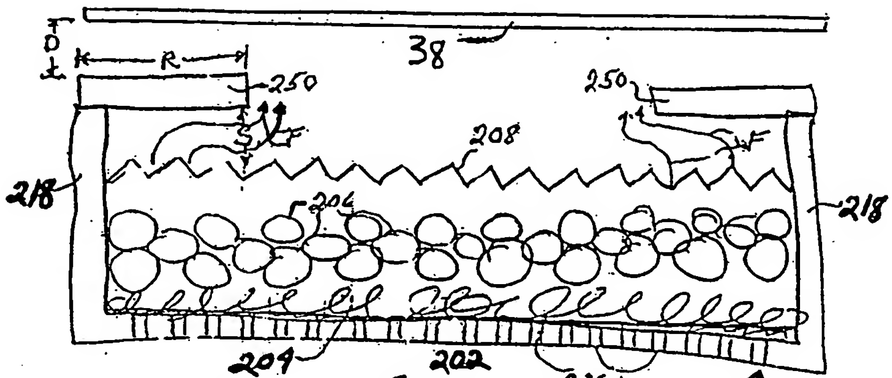

FIG 6

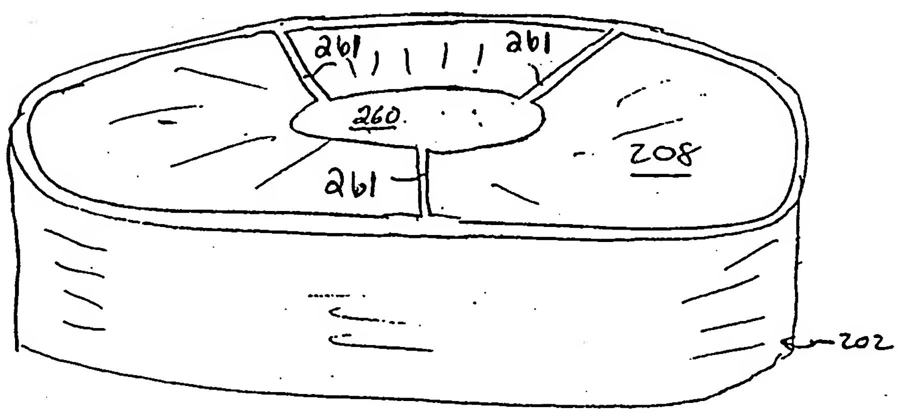

FIG 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/22828

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :C25D 5/00; C25D 17/10
US CL :205/96, 118, 157; 204/227, 228, 242, DIG 7
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 205/96, 118, 157; 204/227, 228, 242, DIG 7

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 5,776,327 A (BOTTS et al) 07 July 1998, see claims.	1-28

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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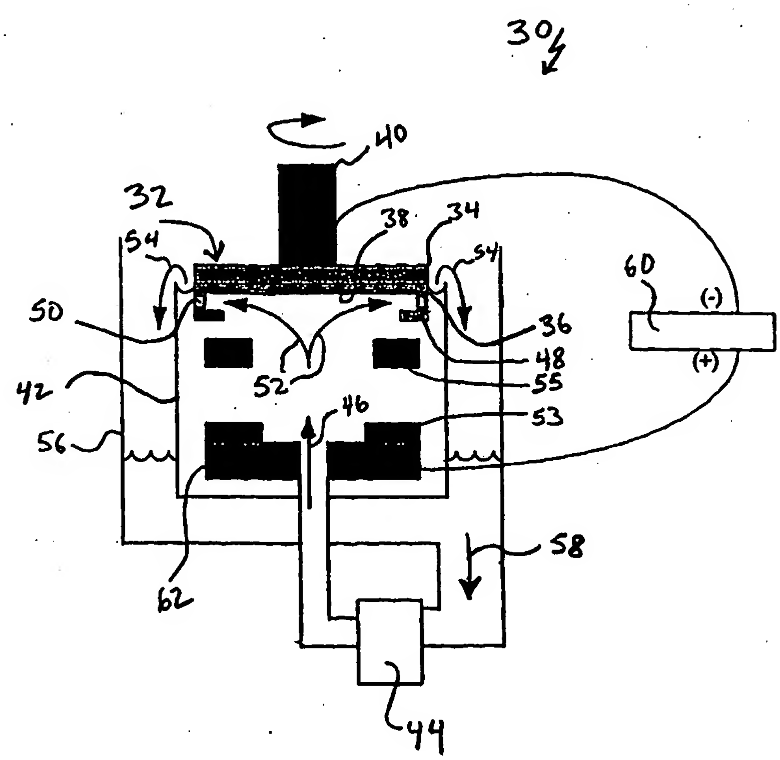
(57) Abstract

Apparatus for treating the surface of a substrate, the apparatus comprising a clamshell (32) mounted on a rotatable spindle (40). The clamshell comprises a cone (34), a cup (36) and a flange (48). The flange (48) has apertures (50) which are adjacent the substrate or wafer (38) allowing gas bubbles entrapped on the substrate surface to readily escape.



ELECTRIC POTENTIAL SHAPING APPARATUS FOR HOLDING A SEMICONDUCTOR WAFER DURING ELECTROPLATING

CROSS REFERENCE TO RELATED APPLICATION

This application is related to Patton et al., co-filed Application Serial No. [Attorney Docket No. M-4269 US], Reid et al., co-filed Application Serial No. [Attorney Docket No. M-4275 US], and Reid et al., co-filed Application Serial No. [Attorney Docket No. M-4272 US], all of which are incorporated herein by reference in their entirety.

FIELD OF INVENTION

The present invention relates generally to an apparatus for treating the surface of a substrate and more particularly to an apparatus for electroplating a layer on a semiconductor wafer.

BACKGROUND OF THE INVENTION

The manufacture of semiconductor devices often requires the formation of electrical conductors on semiconductor wafers. For example, electrically conductive leads on the wafer are often formed by

electroplating (depositing) an electrically conductive layer such as copper on the wafer and into patterned trenches.

Electroplating involves making electrical contact with the wafer surface upon which the electrically conductive layer is to be deposited (hereinafter the "wafer plating surface"). Current is then passed through a plating solution (i.e. a solution containing ions of the element being deposited, for example a solution containing Cu^{++}) between an anode and the wafer plating surface (the wafer plating surface being the cathode). This causes an electrochemical reaction on the wafer plating surface which results in the deposition of the electrically conductive layer.

To minimize variations in characteristics of the devices formed on the wafer, it is important that the electrically conductive layer be deposited uniformly (have a uniform thickness) over the wafer plating surface. However, conventional electroplating processes produce nonuniformity in the deposited electrically conductive layer due to the "edge effect" described in Schuster et al., U.S. Patent No. 5,000,827, herein incorporated by reference in its entirety. The edge effect is the tendency of the deposited electrically conductive layer to be thicker near the wafer edge than at the wafer center.

To offset the edge effect, Schuster et al. teaches non-laminar flow of the plating solution in the region near the edge of the wafer, i.e. teaches adjusting the flow characteristics of the plating solution to reduce

the thickness of the deposited electrically conductive layer near the wafer edge. However, the range over which the flow characteristics can be adjusted is limited and difficult to control. Thus, it is desirable to have a method of offsetting the edge effect which does not rely on adjustment of the flow characteristics of the plating solution.

Another conventional method of offsetting the edge effect is to make use of "thieves" adjacent the wafer. By passing electrical current between the thieves and the anode during the electroplating process, electrically conductive material is deposited on the thieves which otherwise would have been deposited on the wafer plating surface near the wafer edge where the thieves are located. This improves the uniformity of the deposited electrically conductive layer on the wafer plating surface. However, since electrically conductive material is deposited on the thieves, the thieves must be removed periodically and cleaned adding to the maintenance cost and downtime of the apparatus. Further, additional power supplies must be provided to power the thieves adding to the capital cost of the apparatus. Accordingly, it is desirable to avoid the use of thieves.

Nonuniformity of the deposited electrically conductive layer can also result from entrapment of air bubbles on the wafer plating surface. The air bubbles disrupt the flow of ions and electrical current to the wafer plating surface creating nonuniformity in the deposited electrically conductive layer. One

conventional method of reducing air bubble entrapment is to immerse the wafer vertically into the plating solution. However, mounting the wafer vertically adds complexity and hinders automation of the electroplating process. Accordingly, it is desirable to have an apparatus for electroplating a wafer which allows the wafer to be immersed horizontally into the plating solution and yet avoids air bubble entrapment.

SUMMARY OF THE INVENTION

In accordance with the present invention, an apparatus for depositing an electrically conductive layer on the surface of a substrate such as a wafer comprises a flange. The flange has a cylindrical wall and an annulus extending inward from the cylindrical wall, the annulus having an inner perimeter which defines a flange central aperture. The apparatus also includes a cup for supporting the wafer along a peripheral region thereof. The cup has a cup central aperture defined by an inner perimeter of the cup, the cup being positioned above the flange.

In one embodiment, the diameter of the flange central aperture is less than the diameter of the cup central aperture. The annulus of the flange thus extends under the edge region of the wafer surface and reduces the electric current flux to this edge region during electroplating. This, in turn, reduces the thickness of the deposited electrically conductive layer on the edge region of the wafer surface. Of importance, the thickness of the deposited electrically

conductive layer on the edge region of the wafer surface is reduced without the use of thieves.

The thickness of the deposited electrically conductive layer on the edge region of the wafer can be varied by adjusting the diameter of the flange central aperture. To further decrease the thickness of the layer in this region, the diameter of the flange central aperture is decreased; conversely, to increase the thickness of the layer, the diameter is increased. Thus, the thickness profile of the deposited electrically conductive layer across the wafer surface can be readily adjusted by simply modifying the diameter of the flange central aperture.

The flange can further include a plurality of apertures extending through the cylindrical wall of the flange. By locating these apertures adjacent the cup and near the edge region of the wafer surface, air bubbles entrapped on the wafer surface can readily escape through the apertures. To further enhance removal of entrapped air bubbles, the wafer can be rotated while the plating solution is directed towards the center of the wafer surface.

By modifying the width of the apertures in the cylindrical wall of the flange, the electric current flux at the edge region of the wafer surface is adjusted. This, in turn, adjusts the thickness of the deposited electrically conductive layer on the edge region of the wafer surface. Thus, the thickness profile of the deposited electrically conductive layer across the wafer surface can also be readily adjusted

by simply modifying the width of the apertures in the cylindrical wall of the flange.

In accordance with another embodiment of the present invention, a method of depositing an electrically conductive layer on the wafer surface includes providing a cup attached to a flange, the cup having an inner perimeter which defines a cup central aperture, the flange having an annulus. The wafer is then mounted in the cup so that the wafer surface is exposed through the cup central aperture. The cup and flange are then placed into a plating solution, the plating solution contacting the wafer surface. An electrical field and electric current flux is then produced between the wafer surface and an anode in the plating solution wherein the annulus of the flange shapes the electric current flux and reduces the thickness of the deposited electrically conductive layer on the edge region of the wafer surface.

These and other objects, features and advantages of the present invention will be more readily apparent from the detailed description of the preferred embodiments set forth below taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatical view of an electroplating apparatus having a wafer mounted therein in accordance with the present invention.

FIGS. 2A and 2B are cross-sectional views of a cup having a wafer mounted therein illustrating

equipotential surfaces and electric current flux lines, respectively, during electroplating in accordance with the related art.

FIGS. 3A and 3B are cross-sectional views of a flange and a cup having a wafer mounted therein illustrating equipotential surfaces and electric current flux lines, respectively, during electroplating in accordance with the present invention.

FIGS. 4, 5, 6 and 7 are cross-sectional views of cups formed integrally with various flanges in accordance with alternative embodiments of the present invention.

FIGS. 8 and 9 are graphs of the plated thickness versus distance from the wafer center for various flanges in accordance with the present invention.

FIGS. 10A and 10B are top and bottom perspective views, respectively, of a cup formed integrally with a flange in accordance with the present invention.

FIG. 11 is a top plan view, partially in section, of the cup and flange of FIGS. 10A and 10B in accordance with this embodiment of the present invention.

FIG. 12 is a cross-sectional view of the cup and flange taken along the line XII-XII of FIG. 11 in accordance with this embodiment of the present invention.

FIG. 13 is a detailed cross-sectional view of a portion XIII from FIG. 12 of the cup and flange in accordance with this embodiment of the present invention.

FIG. 14 is a top perspective view of a flange in accordance with an alternative embodiment of the present invention.

FIG. 15 is a top plan view of the flange of FIG. 14 in accordance with this embodiment of the present invention.

FIG. 16 is a cross-sectional view of the flange taken along the line XVI - XVI of FIG. 15 in accordance with this embodiment of the present invention.

FIG. 17 is a cross-sectional view of the flange taken along the line XVII - XVII of FIG. 15 in accordance with this embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Several elements in the following figures are substantially similar. Therefore similar reference numbers are used to represent similar elements.

FIG. 1 is a diagrammatical view of an electroplating apparatus 30 having a wafer 38 mounted therein in accordance with the present invention. Apparatus 30 includes a clamshell 32 mounted on a rotatable spindle 40 which allows rotation of clamshell 32. Clamshell 32 comprises a cone 34, a cup 36 and a flange 48. Flange 48 has formed therein a plurality of apertures 50. A clamshell lacking a flange 48 yet in other regards similar to clamshell 32 is described in detail in Patton et al., co-filed Application Serial No. [Attorney Docket No. M-4269], cited above.

During the electroplating cycle, wafer 38 is mounted in cup 36. Clamshell 32 and hence wafer 38 are then placed in a plating bath 42 containing a plating solution. As indicated by arrow 46, the plating solution is continually provided to plating bath 42 by a pump 44. Generally, the plating solution flows upwards to the center of wafer 38 and then radially outward and across wafer 38 through apertures 50 as indicated by arrows 52. Of importance, by directing the plating solution towards the center of wafer 38, any gas bubbles entrapped on wafer 38 are quickly removed through apertures 50. Gas bubble removal is further enhanced by rotating clamshell 32 and hence wafer 38.

The plating solution then overflows plating bath 42 to an overflow reservoir 56 as indicated by arrows 54. The plating solution is then filtered (not shown) and returned to pump 44 as indicated by arrow 58 completing the recirculation of the plating solution.

A DC (or pulsed) power supply 60 has a negative output lead electrically connected to wafer 38 through one or more slip rings, brushes and contacts (not shown). The positive output lead of power supply 60 is electrically connected to an anode 62 located in plating bath 42. During use, power supply 60 biases wafer 38 to have a negative potential relative to anode 62 causing an electrical current to flow from anode 62 to wafer 38. (As used herein, electrical current flows in the same direction as the net positive ion flux and opposite the net electron flux.) This causes an

electrochemical reaction (e.g. $Cu^{++} + 2e^{-} = Cu$) on wafer 38 which results in the deposition of the electrically conductive layer (e.g. copper) on wafer 38. The ion concentration of the plating solution is replenished during the plating cycle, for example by dissolving a metallic anode (e.g. $Cu = Cu^{++} + 2e^{-}$). Shields 53 and 55 are provided to shape the electric field between anode 62 and wafer 38. The use and construction of anodes and shields are further described in Reid et al., co-filed Application Serial No. [Attorney Docket No. M-4272 US] and Reid et al., co-filed Application Serial No. [Attorney Docket No. M-4275 US], both cited above.

FIGS. 2A and 2B are cross-sectional views of a cup 70 having a wafer 38 mounted therein illustrating equipotential surfaces and electric current flux lines, respectively, during electroplating in accordance with the related art. A cup similar to cup 70 is described in detail in Patton et al., co-filed Application Serial No. [Attorney Docket No. M-4269], cited above. For purposes of clarity, the plating solution and anode are not illustrated in FIGS. 2A and 2B but it is understood that cup 70 including wafer 38 is immersed in a plating solution and that an electrical potential (a voltage differential) exists between a conventional electrically conductive seed layer 74 on a plating surface 76 of wafer 38 and the anode (See anode 62 in FIG. 1). Copper on titanium nitride or on tantalum are examples of suitable electrically conductive seed layers.

Referring to FIGS. 2A and 2B, cup 70 is fitted with a compliant seal 72 which forms a seal between cup 70 and plating surface 76. Electrical contacts 78 make the electrical connection with seed layer 74 (electrical contacts 78 are electrically connected to the negative output of a power supply, e.g. see power supply 60 of FIG. 1). By forming a seal between cup 70 and plating surface 76, compliant seal 72 prevents the plating solution from entering a region 77 and contaminating contacts 78, wafer edge 84 and wafer backside 86.

In FIG. 2A, equipotential surfaces V1, V2, V3, V4, V5 and V6 represent surfaces of constant electrical potential within the plating solution. Since seed layer 74 is biased with a negative potential compared to the anode, equipotential surface V1 has the most negative potential and the electrical potential increases (becomes less negative) from equipotential surface V1 to equipotential surface V6.

As shown in FIG. 2A, under central region 80 of plating surface 76 of wafer 38, equipotential surfaces V1 through V6 are substantially parallel to one another demonstrating the uniformity of the electric current flux under central region 80. However under edge region 82 of plating surface 76 of wafer 38 (directly adjacent compliant seal 72), equipotential surface V1 to V6 are bunched together and are moved upwards towards wafer 38 demonstrating nonuniformity of the electric current flux under edge region 82.

Referring now to FIG. 2B, electric current flux lines I1 to I10 are illustrated, although for clarity only flux lines I1, I5 and I10 are labeled. The density of the flux lines at any particular region (the number per unit area perpendicular to the flux lines) is proportional to the magnitude of the electric current flux at the particular region. As shown in FIG. 2B, the spacing between flux lines I5 to I10 under central region 80 is substantially uniform as is the magnitude of the electric current flux. However flux lines I1 to I5 under edge region 82 are spaced closer together than flux lines I5 to I10 indicating that the magnitude of the electric current flux under edge region 82 is greater than under central region 80. Flux lines I1 to I5 are spaced together since cup 70 is formed of, or alternatively coated with, a dielectric which shapes the electric current flux. Since the electric current flux per unit area is proportional to the number of flux lines entering the unit area, the electric current flux per unit area of edge region 82 is greater than the electric current flux per unit area of central region 80. Since the amount of electrically conductive material deposited per unit area is directly related to the electric current flux per unit area, the thickness of the electrically conductive layer deposited on plating surface 76 is thickest on edge region 82.

FIGS. 10A and 10B are top and bottom perspective views, respectively, of a cup 36F formed integrally with a flange 48F in accordance with the one embodiment

of the present invention. As best shown in FIG. 10B, flange 48F comprises a vertical cylindrical wall 51F and an annulus 49F. More particularly, a first end of wall 51F is integrally attached to cup 36F and a second end of wall 51F is integrally attached to annulus 49F. Extending from the inner cylindrical surface to the outer cylindrical surface of wall 51F are a plurality of apertures 50F which are circular holes. The advantages of flange 48F are similar to the advantages discussed below in regards to flange 48A of FIGS. 3A and 3B.

FIGS. 3A and 3B are cross-sectional views of a cup 36A having a wafer 38 mounted therein and a flange 48A integral with cup 36A illustrating equipotential surfaces and electric current flux lines, respectively, during electroplating in accordance with the present invention. For purposes of clarity, the plating solution and anode are not illustrated in FIGS. 3A and 3B but it is understood that cup 36A including wafer 38 and flange 48A are immersed in a plating solution and that an electrical potential exists between seed layer 74 and the anode.

In accordance with this embodiment, flange 48A includes an annulus 49A which horizontally extends inward beyond inner perimeter 90 of cup 36A. Thus, annulus 49A has an inner perimeter 92 which defines a flange central aperture having a diameter less than the cup central aperture defined by inner perimeter 90 of cup 36A. Flange 48A and cup 36A are formed from a dielectric material or alternatively, from an

electrically conductive material have an insulative coating. For example, flange 48A and cup 36A are formed of an electrically insulating material such as polyvinylidene fluoride (PVDF) or chlorinated polyvinyl chloride (CPVC). Instead of forming flange 48A integrally with cup 36A, flange 48A can also be formed separately from cup 36A and then attached to cup 36A. For example, flange 48A can be bolted to cup 36A.

Extending horizontally (substantially parallel to the plane defined by inner perimeter 90 of cup 36A) and through a vertical cylindrical wall 51A of flange 48A are a plurality of apertures 50A. By locating apertures 50A adjacent cup 36A and near edge region 82 of plating surface 76, any gas bubbles entrapped on plating surface 76 are readily released through apertures 50A.

Referring to FIG. 3A, equipotential surfaces V11, V12, V13, V14, V15 and V16 representing surfaces of constant electric potential within the plating solution are illustrated. Equipotential surface V11 has the most negative potential and the electrical potential increases from equipotential surface V11 to equipotential surface V16. The substantially uniform spacing between equipotential surfaces V11 to V16 demonstrates the uniformity of the electric current flux near wafer 38. Of importance, the equipotential surfaces V11, V12 and V13 have substantially uniform spacing under both edge region 82 and central region 80 thus demonstrating the uniformity of the electric current flux in these regions.

Referring now to FIG. 3B, electric current flux lines I11 to I20 are illustrated although for clarity only flux lines I11, I12, I18 and I20 are labeled. As shown in FIG. 3B, the spacing between flux lines I12 to I18 is reduced adjacent inner perimeter 92 of annulus 49A indicating a greater magnitude of the electric current flux in this region. However, flux lines I12 to I18 spread from annulus 49A to plating surface 76 and are substantially uniformly spaced at plating surface 76. Flux line I11 extends through aperture 50A thus contributing to the magnitude of the electric current flux at edge region 82. Flux lines I18 to I20 are uniformly spaced from one another and are substantially unaffected by annulus 49A and cup 36A.

Of importance, flux lines I11 to I20 are substantially uniformly spaced at plating surface 76 in both edge region 82 and central region 80. Thus the magnitude of the electric current flux at plating surface 76 is uniform. Since the amount of electrically conductive material deposited per unit area of plating surface 76 is directly related to the electric current flux per the unit area, the thickness of the deposited electrically conductive layer on plating surface 76 is substantially uniform. In one embodiment, the thickness uniformity of the deposited electrically conductive layer is within 2%, i.e. the thickness of the deposited electrically conductive layer at any given point is within 2% of the average thickness of the deposited electrically conductive layer.

FIGS. 4, 5, 6 and 7 are cross-sectional views of cups formed integrally with various flanges in accordance with alternative embodiments of the present invention. For clarity, the cones (see cone 34 of FIG. 1) are not illustrated in FIGS. 4, 5, 6 and 7.

Referring to FIG. 4, a wafer 38 is mounted in a cup 36B. Wafer 38 is pressed down on to compliant seal 72B by a cone (not shown). This forms the electrical connection between contacts 78B and seed layer 74 on plating surface 76. As shown in FIG. 4, cup 36B has an inner perimeter 90B which defines a cup central aperture A_{CB} having a diameter ID_{CB}. Flange 48B has an annulus 49B having an inner perimeter 92B which defines a flange central aperture A_{FB} having a diameter ID_{FB}. Since diameter ID_{FB} is less than diameter ID_{CB}, annulus 49B extends under the edge region of plating surface 76 effectively shielding the edge region, i.e. flange 48B reduces the electric current flux to the edge region of plating surface 76. This, in turn, reduces the thickness of the deposited electrically conductive layer on the edge region of plating surface 76.

Referring now to FIG. 5, cup 36C is substantially similar to cup 36B (FIG. 4). However, in the FIG. 5 embodiment, the annulus 49C of flange 48C extends further under the edge region towards the center of plating surface 76 than does annulus 49B (FIG. 4). Thus, flange 48C shields more of the edge region of plating surface 76 than does flange 48B.

FIG. 8 is a graph of the resulting thickness in microns (μm) of the deposited electrically conductive

layer (the "plated thickness") versus distance in millimeters (mm) from the center of wafer 38 for flanges 48B and 48C in accordance with the present invention. More particularly, trace 100B is for flange 48B (FIG. 4) where the inner diameter ID_{FB} of annulus 49B is 7.33 inch (18.62 cm.) and trace 102C is for flange 48C (FIG. 5) where the inner diameter ID_{FC} of annulus 49C is 7.13 in. (18.11 cm.). As shown in FIG. 8, the plated thickness gradually increases from about 1.32 µm at the wafer center to about 1.73 µm at about 80 mm from the wafer center in both traces 100B and 102C. The plated thickness for trace 102C then decreases to about 1.35 µm at about 93 mm from the wafer center. This abrupt falloff of plated thickness at the edge region results from the relatively large shielding effect of flange 48C. In contrast, the plated thickness for trace 100B decreases only slightly from about 1.78 µm at about 87 mm from the wafer center to about 1.65 µm at about 93 mm from the wafer center. Without flanges 48B, 48C, traces 100B, 102C, respectively, would not fall off (would not have a negative slope) at the edge region of the wafer.

As shown by traces 102C, 100B, the plated thickness profile across the plating surface is readily adjusted by simply modifying the inner diameter of the flange. More particularly, by decreasing the inner diameter of the flange the plated thickness on the edge region is reduced; conversely, by increasing the inner diameter of the flange the plated thickness of the edge region is increased.

Referring now to FIG. 6, cup 36D is substantially similar to cup 36B (FIG. 4). However, in the FIG. 6 embodiment, the width W_{HD} of apertures 50D extending through flange 48D is greater than the width W_{HB} of apertures 50B extending through flange 48B. Forming flange 48D with apertures 50D having a greater width W_{HD} increases the electric current flux through apertures 50D (see flux line I11 in FIG. 3B). Increasing the electric current flux results in a greater plating thickness on the edge region of wafer plating surface 76.

FIG. 9 is a graph of the resulting plated thickness in microns versus distance in millimeters from the center of wafer 38 for flanges 48B and 48D in accordance with the present invention. More particularly, trace 110B is for flange 48B (FIG. 4) having apertures 50B with widths W_{HB} equal to 0.05 in. (0.13 cm.) and trace 112D is for flange 48D (FIG. 6) having apertures 50D with widths W_{HD} equal to 0.10 in. (0.25 cm.).

As shown in FIG. 9, at about 85 mm from the wafer center the plating thickness of trace 110B decreases abruptly from about 1.68 μm to about 1.42 μm at about 93 mm from the wafer center due to the shielding of the edge region of plating surface 76 from flange 48B. In contrast, as shown by trace 112D, the plating thickness only decreases slightly over this same edge region from approximately 1.67 μm to 1.62 μm due to the increased electric current flux through apertures 50D. (Note that the anode to wafer spacing was greater by

approximately 1.0 cm in FIG. 8 than in FIG. 9 thus accounting for the differences in traces 100B, 110B of FIGS. 8, 9, respectively.)

Thus, as shown by traces 110B, 112D in FIG. 9, the plated thickness profile across the plating surface is readily adjusted by simply modifying the width of the apertures in the flange. More particularly, by increasing the width of the apertures in the flange the plated thickness on the edge region is increased; conversely, by decreasing the width of the apertures in the flange the plated thickness on the edge region is decreased. This is a significant advantage over the prior art in which the severe limitations of adjusting the flow characteristics of the plating solution limits adjustment of the plated thickness profile.

Referring again to FIGS. 4, 5 and 6, annuluses 49B, 49C and 49D have inner perimeters 92B, 92C and 92D which are surfaces perpendicular to the planes defined by flange central apertures A_{FB}, A_{FC}, A_{FD}, respectively (i.e. inner perimeters 92B, 92C and 92D are perpendicular to the plane defined by wafer plating surface 76). In contrast, referring now to FIG. 7, annulus 49E of flange 48E has an inner perimeter 92E sloped relative to the plane defined by flange central aperture A_{FE}. More particularly, inner perimeter 92E flares inward from a first diameter equal to inner diameter ID_{CE} of inner perimeter 90E of cup 36E to a second lesser diameter ID_{FE}. This embodiment results in a less abrupt change in the plating thickness at the

edge region of plating surface 76 compared to flanges 48B, 48C and 48D of FIGS. 4, 5 and 6, respectively.

FIGS. 10A and 10B are top and bottom perspective views, respectively, of a cup 36F formed integrally with a flange 48F in accordance with another embodiment of the present invention. As shown in FIG. 10A, cup 36F has an inner perimeter 90F which defines a cup central aperture A_{CF}. Threaded bolt holes 120 are provided in cup 36F for bolting one or more contact strips to cup 36F. These contact strips are not illustrated in FIGS. 10A and 10B for purposes of clarity.

Referring now to FIG. 10B, flange 48F comprises a vertical cylindrical wall 51F and an annulus 49F. More particularly, a first end of wall 51F is integrally attached to cup 36F and a second end of wall 51F is integrally attached to annulus 49F. Extending from the inner cylindrical surface to the outer cylindrical surface of wall 51F are a plurality of apertures 50F which are circular holes. Annulus 49F has an inner perimeter 92F which defines a flange central aperture A_{FF}. Flange central aperture A_{FF} has a diameter less than the diameter of cup central aperture A_{CF} (FIG. 10A) and less than the inner diameter of wall 51F.

FIG. 11 is a top plan view, partially in section, of cup 36F integral with flange 48F in accordance with the FIGS. 10A and 10B embodiment of the present invention. Cup 36F and flange 48F are formed of an electrically insulating material such as CPVC. Illustrative specifications for various characteristics

of cup 36F and flange 48F shown in FIG. 11 are provided in Table I below.

TABLE I

CHARACTERISTIC	DESCRIPTION	SPECIFICATION
A	registration notch	2X R .158 In. (180° APART)
B	registration notch champfer	45° X 0.50 In. CHAMPFER, 2 PLCS (BOTH SLOTS)
C	alignment pin receptacle	0.138 In. X .390 In. DP. C'SINK 45° X .030 In. DE. 2 PLCS, 180° APART
D	contact mounting holes	DRILL 0.104 In. X .300 In. DP (.340 In. MAX DP. AT DRILL POINT) BOTTOM TAP 6-32 THRD, 24 PLCS
E	registration notch center diameter	10.380 In.
F	alignment pin receptacle diameter	8.860 In.
G	contact strip arc	8X 45.0°
H	contact mounting hole arc angles	22.5°
I	contact mounting hole arc angles	8X 45.0°
J	contact mounting hole arc angles	7.0°

FIG. 12 is a cross-sectional view of cup 36F and flange 48F taken along the line XII-XII of FIG. 11 in accordance with this embodiment of the present invention. Illustrative specifications for various characteristics of cup 36F and flange 48F shown in FIG. 12 are provided in Table II below.

TABLE II

CHARACTERISTIC	DESCRIPTION	SPECIFICATION
K	clamshell OD	09.080 In.
L	wafer seal OD	08.480 In.
M	contact mounting ID	08.280 In.
ID_{CF}	cup central aperture diameter	01.530 In.
ID_{FF}	flange central aperture diameter	07.330 In.
P	cup ID	08.130 In.
Q	cup OD	010.550 In.
R	Inner cup lip height	.150 In.
S	cup lip height	.310 In.
T	contact mounting hole vertical position	.521 In.
U	parallelism	.005 In.

FIG. 13 is a cross-sectional view of a portion XIII from FIG. 12 of cup 36F and flange 48F in accordance with this embodiment of the present invention. Illustrative specifications for various characteristics of cup 36F and flange 48F shown in FIG. 13 are provided in Table III below.

TABLE III

CHARACTERISTIC	DESCRIPTION	SPECIFICATION
V	vent hole diameter	120 PLCS. 3° APART
W	flange height	.353 In.
X	wafer seal relief	R.020 In. X .020 In. DP.
Y	contact relief height	.275 In.
Z	lower cup height	1.111 In.
A1	wafer seal to hole distance	.022 In. REF
B1	hole vertical position	1.005 In.
C1	wafer seal vertical position	.921 In.

Note that all characteristics in Tables I, II and III are symmetrical and must be concentric with the center bore center line within 0.005 total indicated radius in inches (TIR) and that all edges should be lightly deburred.

FIG. 14 is a top perspective view of a flange 48G in accordance with an alternative embodiment of the present invention. Flange 48G is formed from an electrically insulative material such as PVC. Flange 48G comprises a vertical cylindrical wall 51G and an annulus 49G. Wall 51G is provided with holes 140 for mounting flange 48G to a cup (not shown). Bolts are passed through holes 140 and into the cup to mount flange 48G to the cup. This is in contrast to flange 48F of FIGS. 10A, 10B, 11, 12 and 13 which is formed

integrally with cup 36F. Referring still to FIG. 14, wall 51G is formed with four apertures 50G shaped as elongated slots. Directly below apertures 50G and integrally attached to an end of wall 51G is an annulus 49G having an inner perimeter 92G which defines a flange central aperture A_{FG}.

FIG. 15 is a top plan view of flange 48G of FIG. 14 in accordance with this embodiment of the present invention. Illustrative specifications for various characteristics of flange 48G shown in FIG. 15 are provided in Table IV below.

TABLE IV

CHARACTERISTIC	SPECIFICATION
D1	6X 60.0°
E1	4X 10.0°
F1	4X 80.0°
ID_{FG}	7.33 In. OR 7.13 In.
H1	010.00 In.
I1	09.080 In.

FIG. 16 is a cross-sectional view of flange 48G taken along the line XVI - XVI of FIG. 15 in accordance with this embodiment of the present invention. Illustrative specifications for various characteristics of flange 48G shown in FIG. 16 are provided in Table V below.

TABLE V

CHARACTERISTIC	SPECIFICATION
J1	.090 In.
K1	.400 In.
L1	1.00 In.

FIG. 17 is a cross-sectional view of flange 48G taken along the line XVII - XVII of FIG. 15 in accordance with this embodiment of the present invention. Illustrative specifications for various characteristics of flange 48G shown in FIG. 17 are provided in Table VI below.

TABLE VI

CHARACTERISTIC	SPECIFICATION
M1	6X 1/4-20 THRD
N1	.200 In.
O1	.20 In.
P1	5.9°

Having thus described the preferred embodiments, persons skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention. For example, although the substrate is described and illustrated as a circular wafer having an electrically conductive seed layer on the plating surface, any substrate having an electrically conductive layer on a substantially planar surface (such as a wafer having a flat) or any electrically conductive substrate having a substantially planar surface can be treated. Further,

instead of electroplating a layer on a substrate, the system can be used to electrochemically etch or polish a layer on a substrate. Thus the invention is limited only by the following claims.

We Claim:

1. An apparatus for treating a surface of a substrate comprising a flange, said flange having a cylindrical wall and an annulus attached to a first end of said cylindrical wall, said annulus having an inner perimeter which defines a flange central aperture.

2. The apparatus of Claim 1 wherein extending through said cylindrical wall from an inner cylindrical surface to an outer cylindrical surface are one or more apertures.

3. The apparatus of Claim 2 wherein said one or more apertures are circular holes.

4. The apparatus of Claim 2 wherein said one or more apertures are elongated slots.

5. The apparatus of Claim 1 further comprising a cup having a cup central aperture defined by an inner perimeter of said cup.

6. The apparatus of Claim 5 wherein a diameter of said flange central aperture is less than a diameter of said cup central aperture.

7. The apparatus of Claim 5 further comprising a compliant seal adjacent said inner perimeter of said cup.

8. The apparatus of Claim 7 further comprising a plurality of contacts adjacent said compliant seal.

9. The apparatus of Claim 5 wherein said cylindrical wall has one or more threaded bolt holes for attaching said flange to said cup.

10. The apparatus of Claim 5 wherein a second end of said cylindrical wall is attached to said cup.

11. The apparatus of Claim 1 further comprising a spindle for rotating said flange.

12. The apparatus of Claim 1 wherein said flange comprises a dielectric material.

13. The apparatus of Claim 12 wherein said dielectric material is selected from the group consisting of polyvinylidene fluoride (PVDF) and chlorinated polyvinyl chloride (CPVC).

14. The apparatus of Claim 1 wherein said flange comprises an electrically conductive material having an electrically insulative coating thereon.

15. The apparatus of Claim 1 further comprising a plating bath including a plating solution.

16. The apparatus of Claim 15 further comprising a pump for recirculating said plating solution.

17. The apparatus of Claim 15 wherein said plating solution contains ions of an electrically conductive material.

18. The apparatus of Claim 17 wherein said electrically conductive material is copper.

19. The apparatus of Claim 1 further comprising an anode.

20. The apparatus of Claim 19 further comprising a power supply for creating an electrical potential between said substrate and said anode.

21. The apparatus of Claim 1 wherein said inner perimeter of said annulus is a surface perpendicular to the plane defined by said flange central aperture.

22. The apparatus of Claim 1 wherein said inner perimeter of said annulus is a sloped surface relative to the plane defined by said flange central aperture.

23. A method of treating a surface of a substrate comprising the following steps:

providing a cup attached to a flange, said cup having an inner perimeter which defines a cup central aperture, said flange comprising an annulus;

mounting said substrate in said cup so that said substrate surface is exposed through said cup central aperture;

placing said cup and flange into a plating solution, said plating solution contacting said substrate surface; and

producing an electric current flux between said substrate surface and an anode in said plating solution wherein said annulus of said flange shapes said electric current flux.

24. The method of Claim 23 wherein said step of producing an electric current flux comprises producing a voltage differential between said substrate surface and said anode.

25. The method of Claim 23 wherein said annulus reduces the magnitude of the electric current flux at an edge region of said substrate surface adjacent an edge of said substrate.

26. The method of Claim 25 wherein said step of producing an electric current flux causes an electrically conductive layer to be deposited on said substrate surface, said annulus reducing the thickness of said electrically conductive layer on said edge region of said substrate surface.

27. The method of Claim 23 further comprising the step of directing said plating solution towards the center of said substrate surface.

28. The method of Claim 27 wherein said flange comprises a cylindrical wall having one or more apertures therethrough, said plating solution flowing radially outward from said center of said substrate surface and through said one or more apertures.

29. The method of Claim 28 wherein said step of directing said plating solution removes gas bubbles entrapped on said substrate surface through said one or more apertures.

30. The method of Claim 23 further comprising the step of rotating said cup, flange and substrate.

31. The method of Claim 23 wherein said plating solution contains ions of an electrically conductive material..

32. The method of Claim 31 wherein said electrically conductive material is copper.

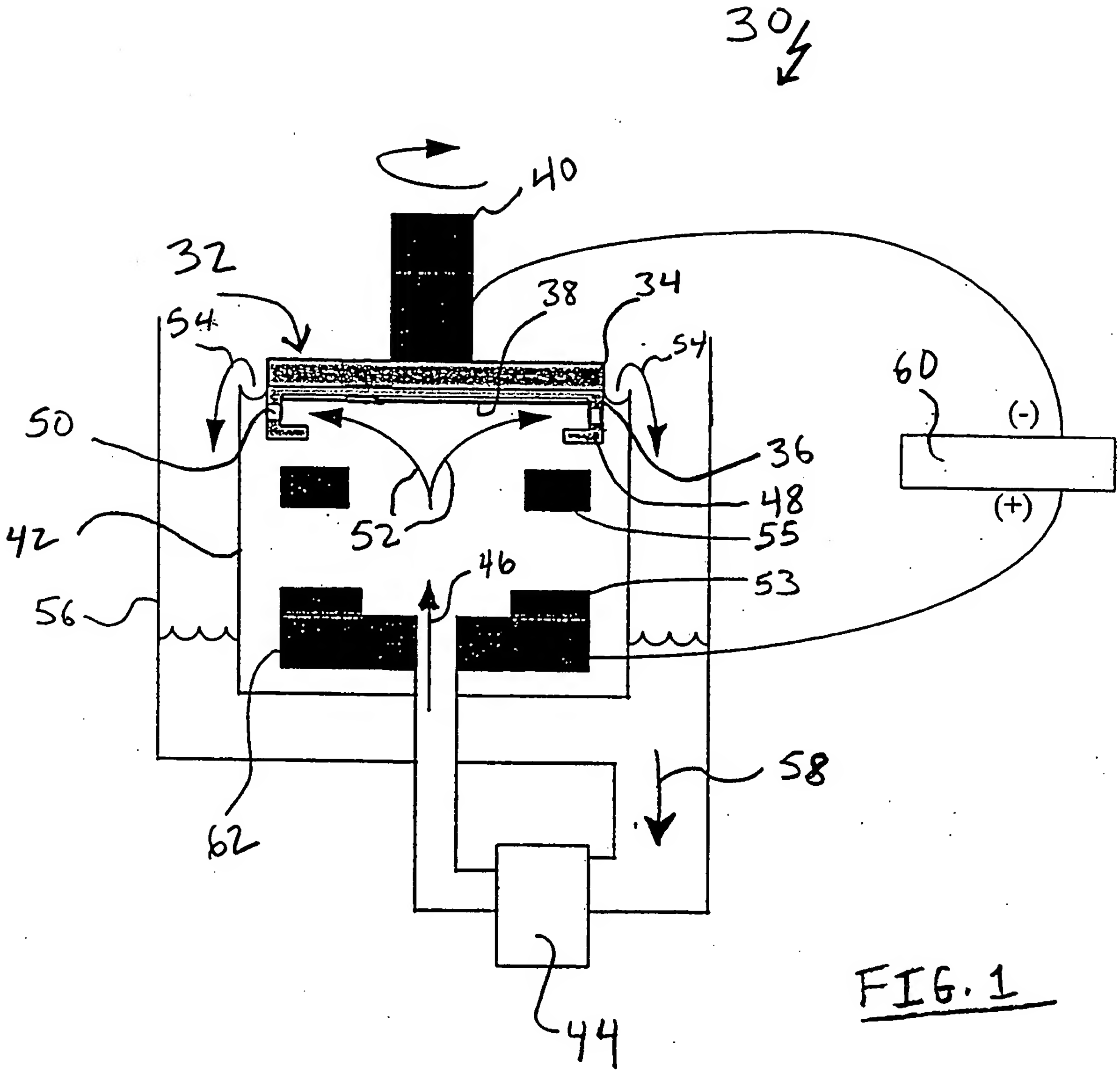
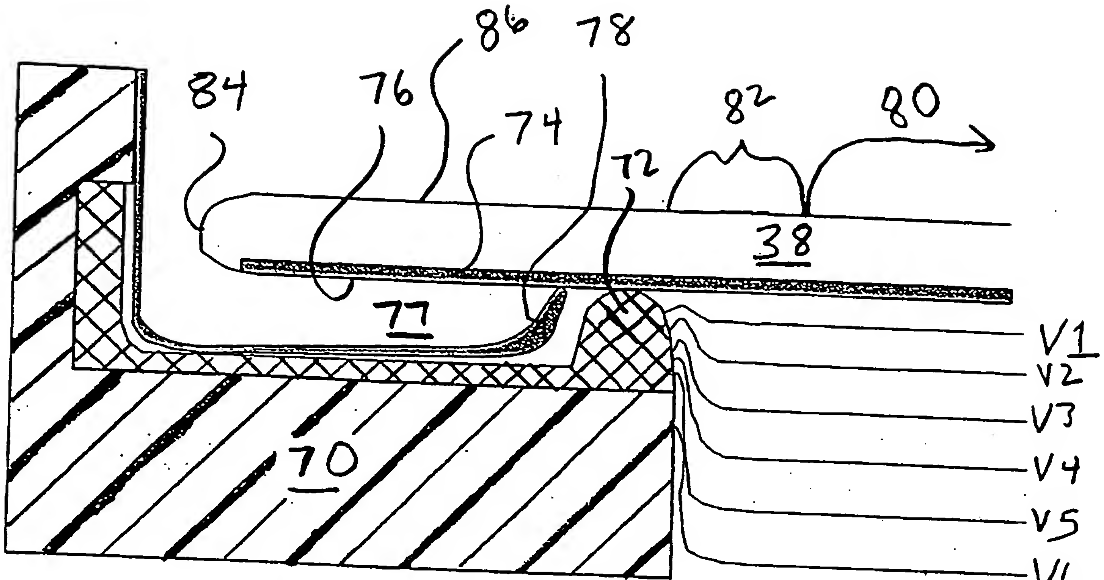


FIG. 1


86
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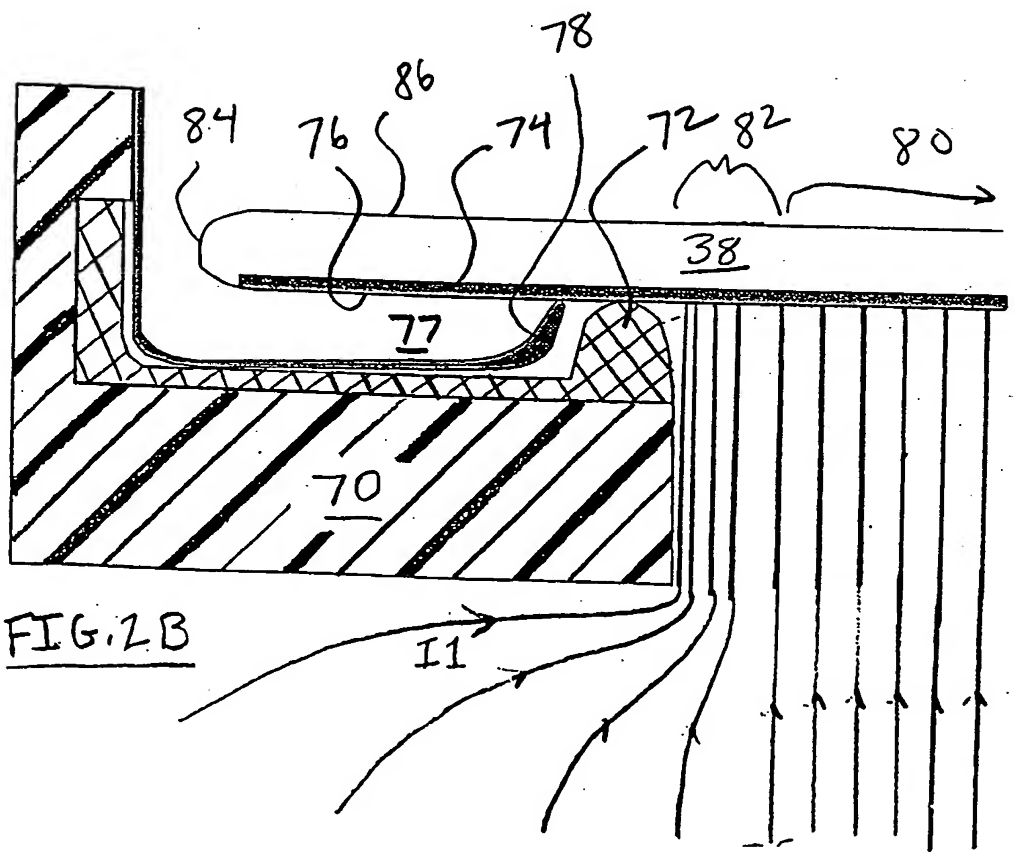
74
82
80
72
38
77
70
V1
V2
V3
V4
V5
V6

FIG. 2A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77
70
I1

FIG. 2B

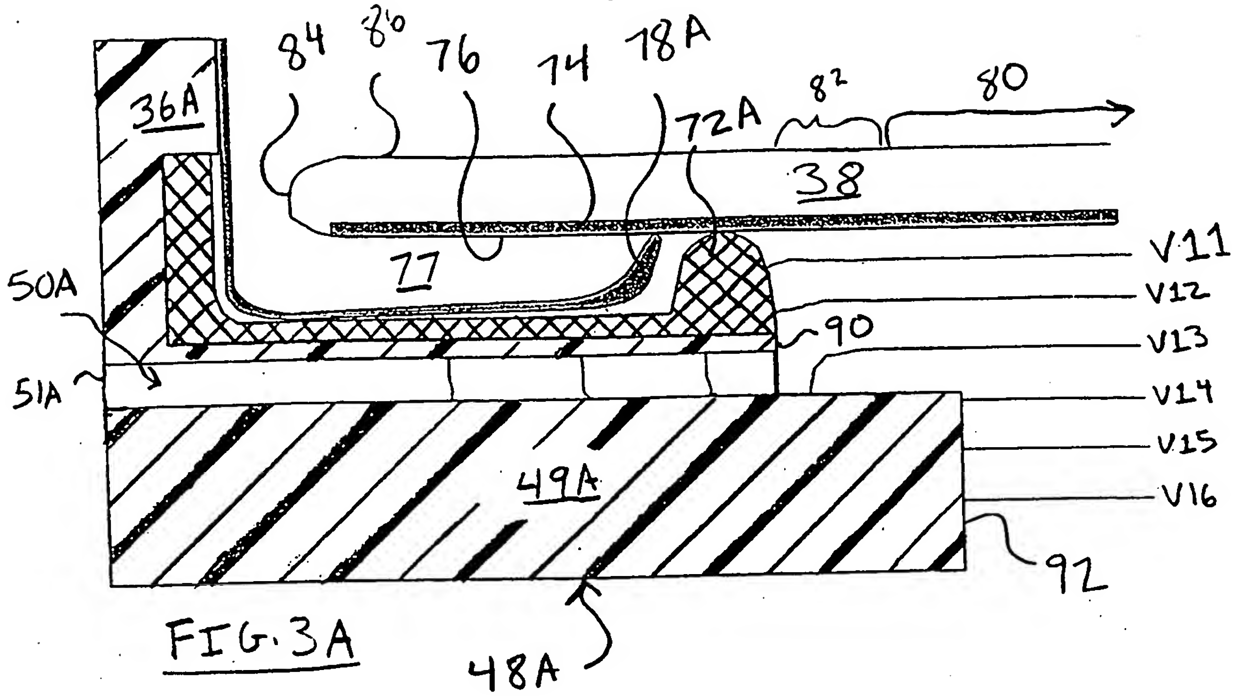

84
86
76
74
78A
82
80
72A
36A
38
77
50A
51A
V11
V12
V13
V14
V15
V16
90
49A
92
48A

FIG. 3A

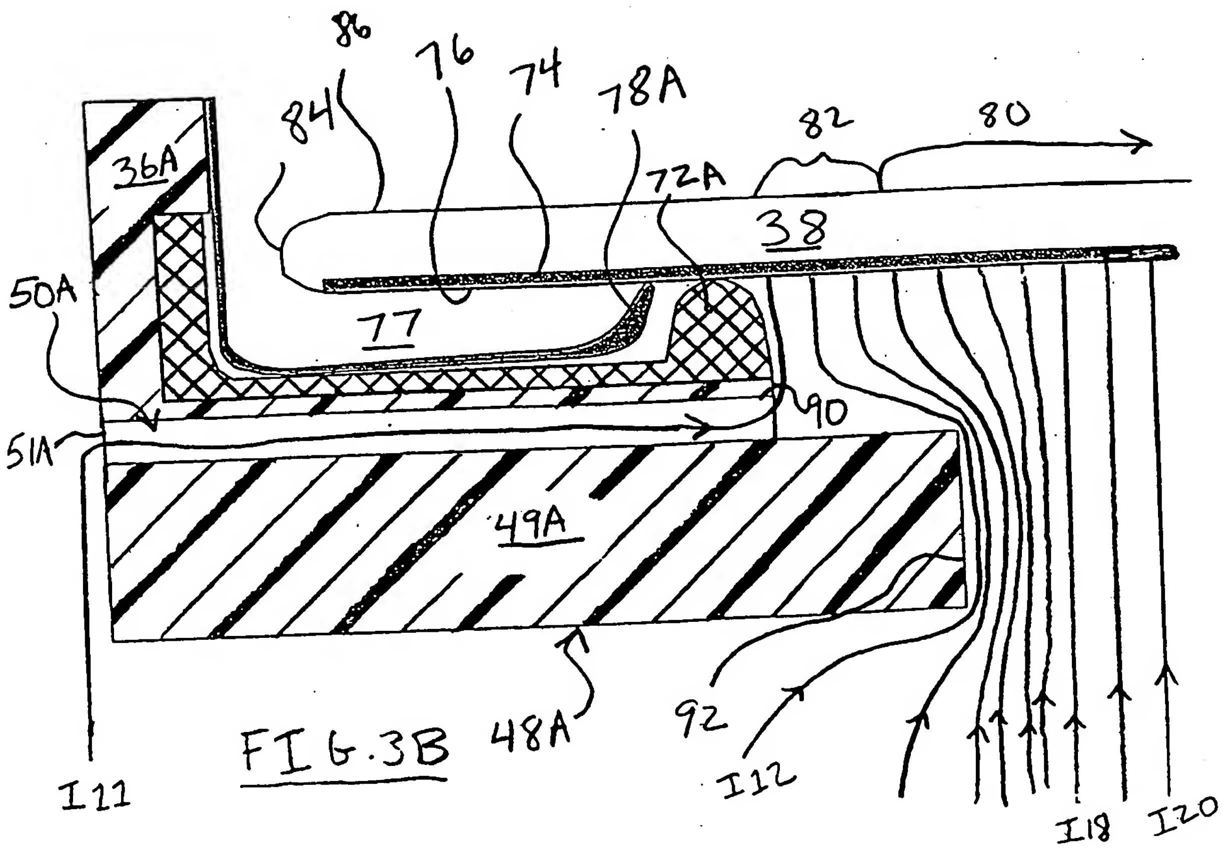

86
76
74
84
78A
82
80
72A
36A
38
50A
77
90
51A
49A
92
48A
I11
I12
I18
I20

FIG. 3B

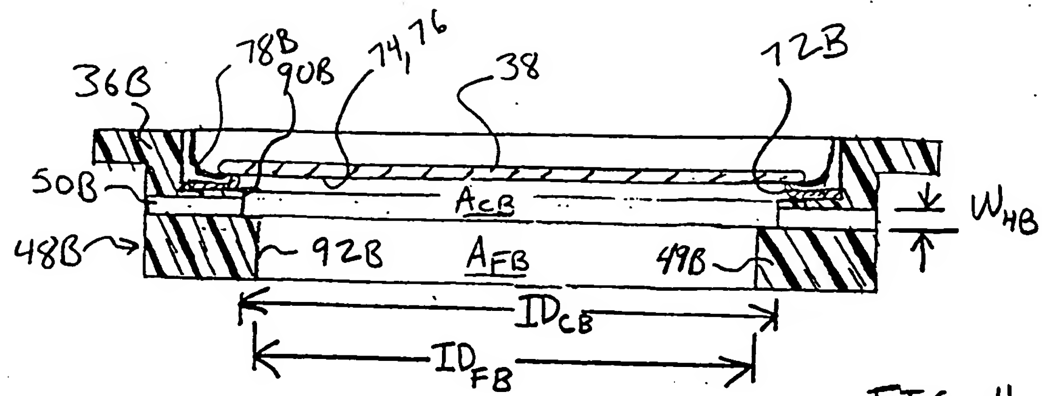


FIG. 4

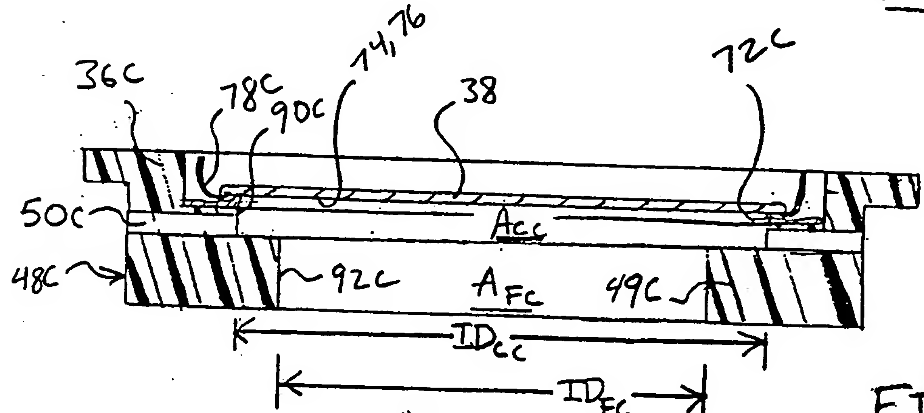


FIG. 5

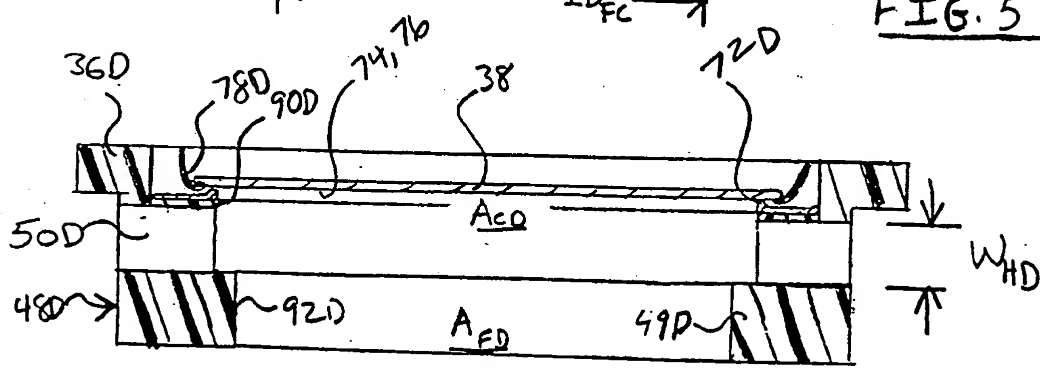


FIG. 6

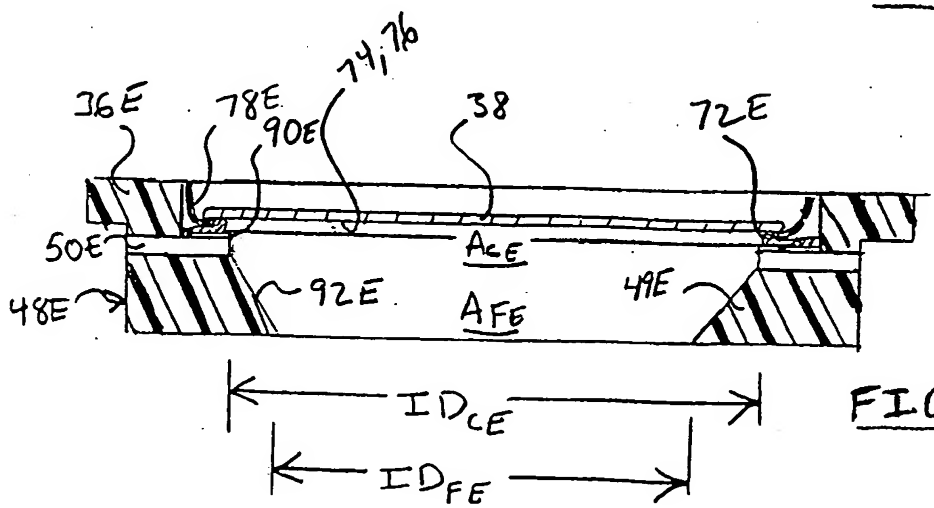
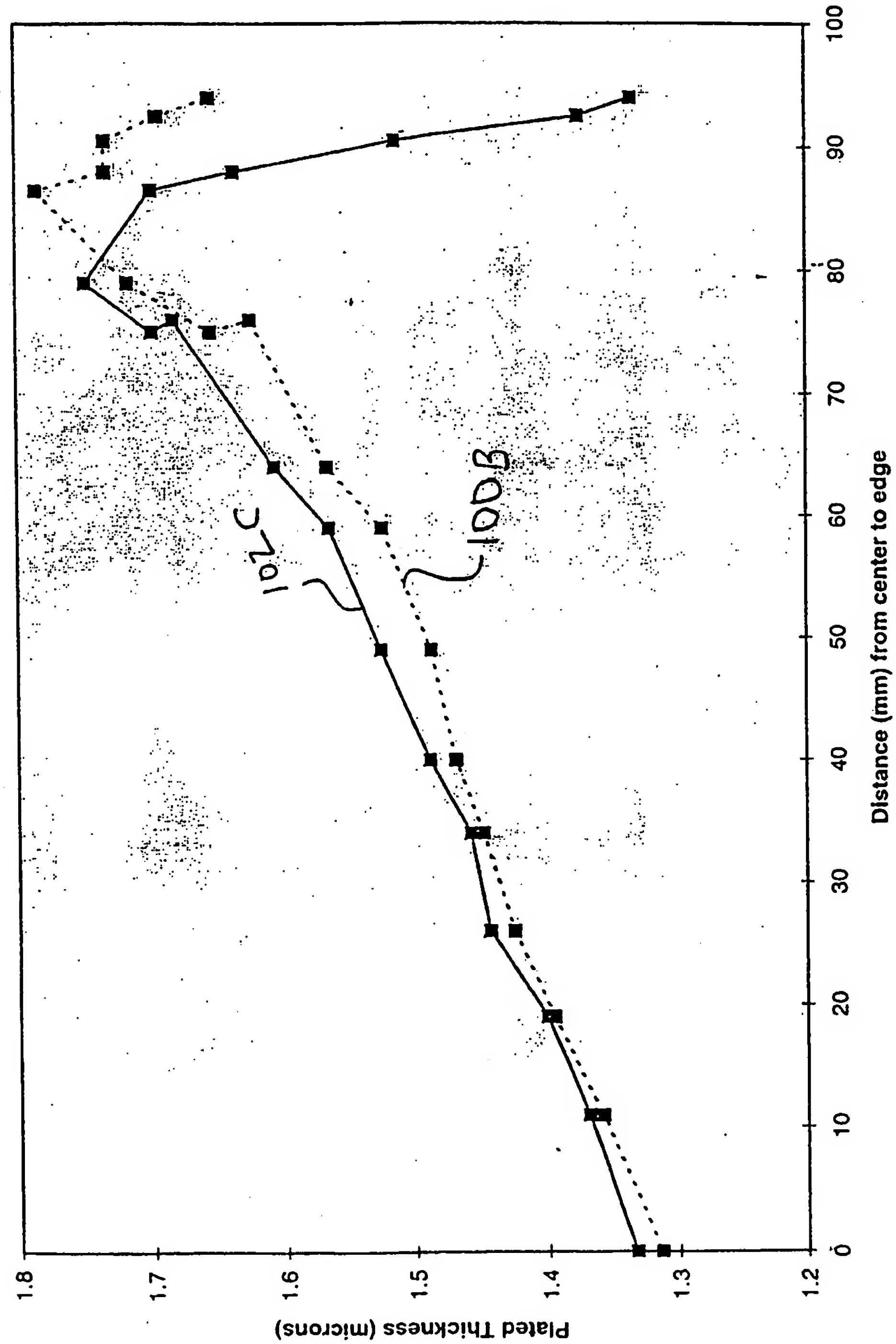


FIG. 7

FIG. 8


Plated Thickness (microns)
1.8
1.7
1.6
1.5
1.4
1.3
1.2
Distance (mm) from center to edge
0
10
20
30
40
50
60
70
80
90
100
102C
100B

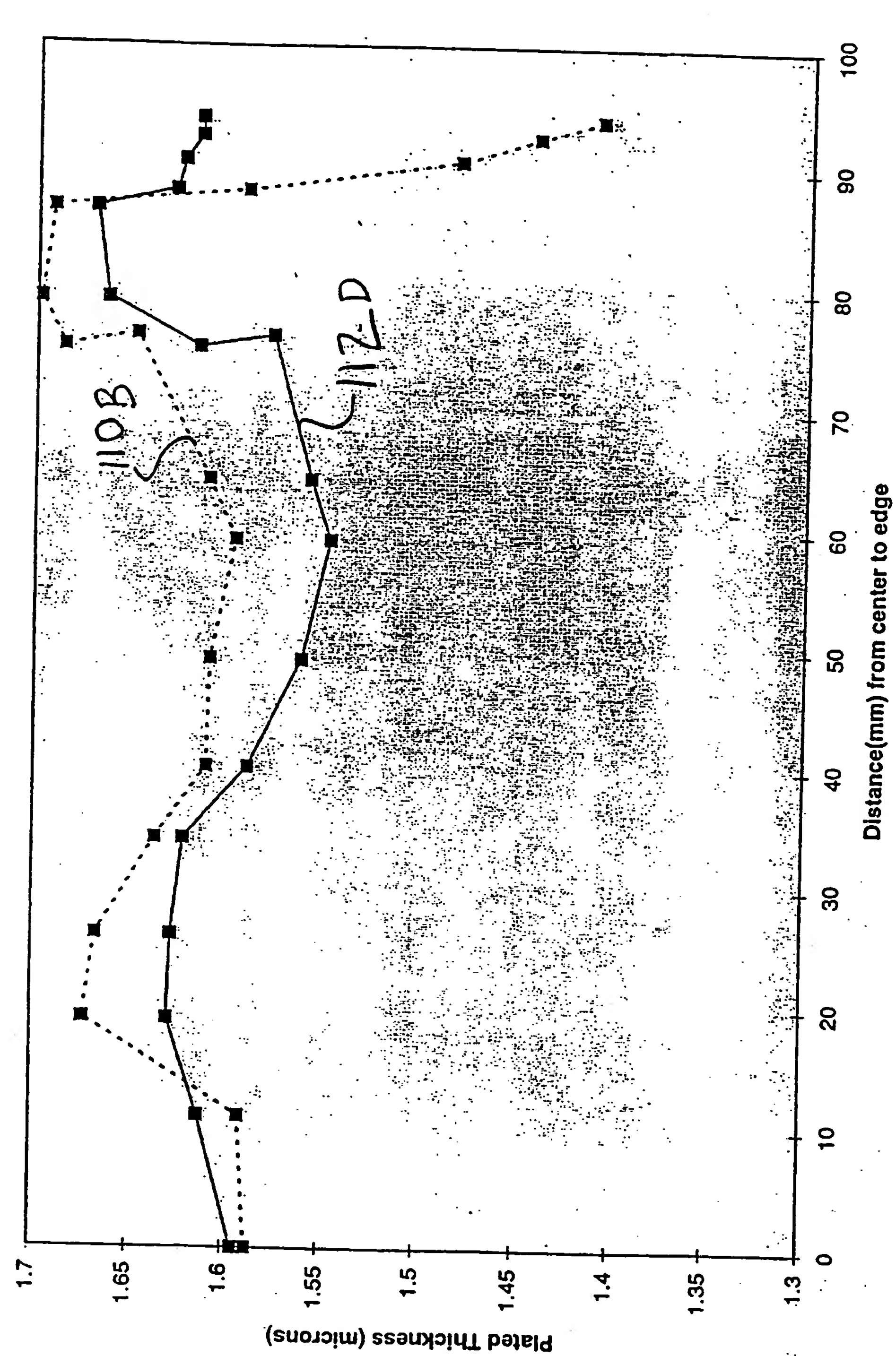

Plated Thickness (microns)
1.7
1.65
1.6
1.55
1.5
1.45
1.4
1.35
1.3
0
10
20
30
40
50
60
70
80
90
100
Distance(mm) from center to edge
110B
112D

FIG. 9

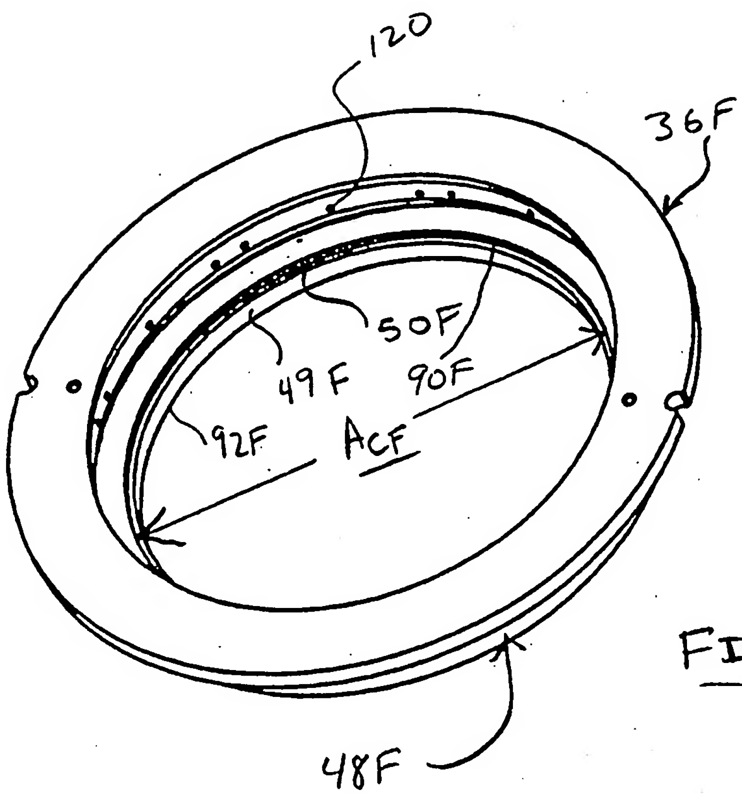


FIG. 10 A

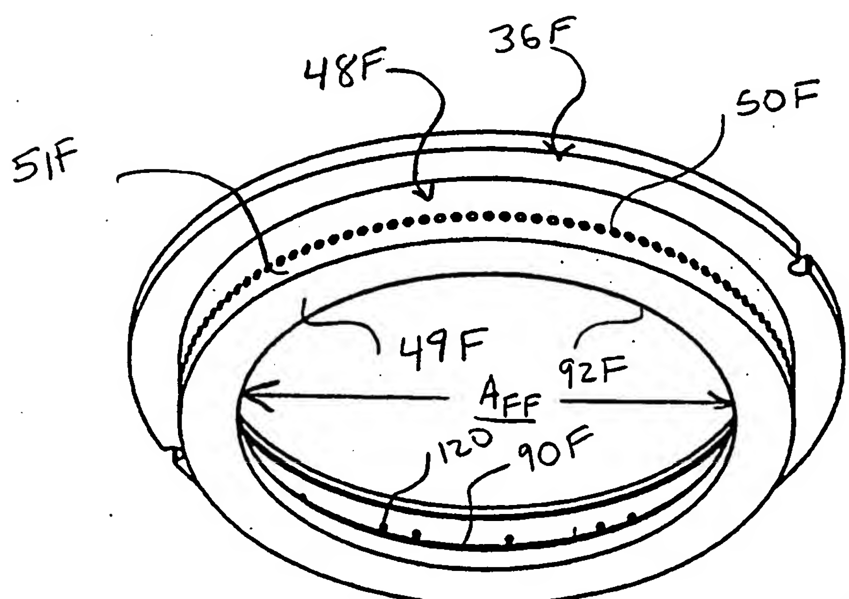


FIG. 10 B

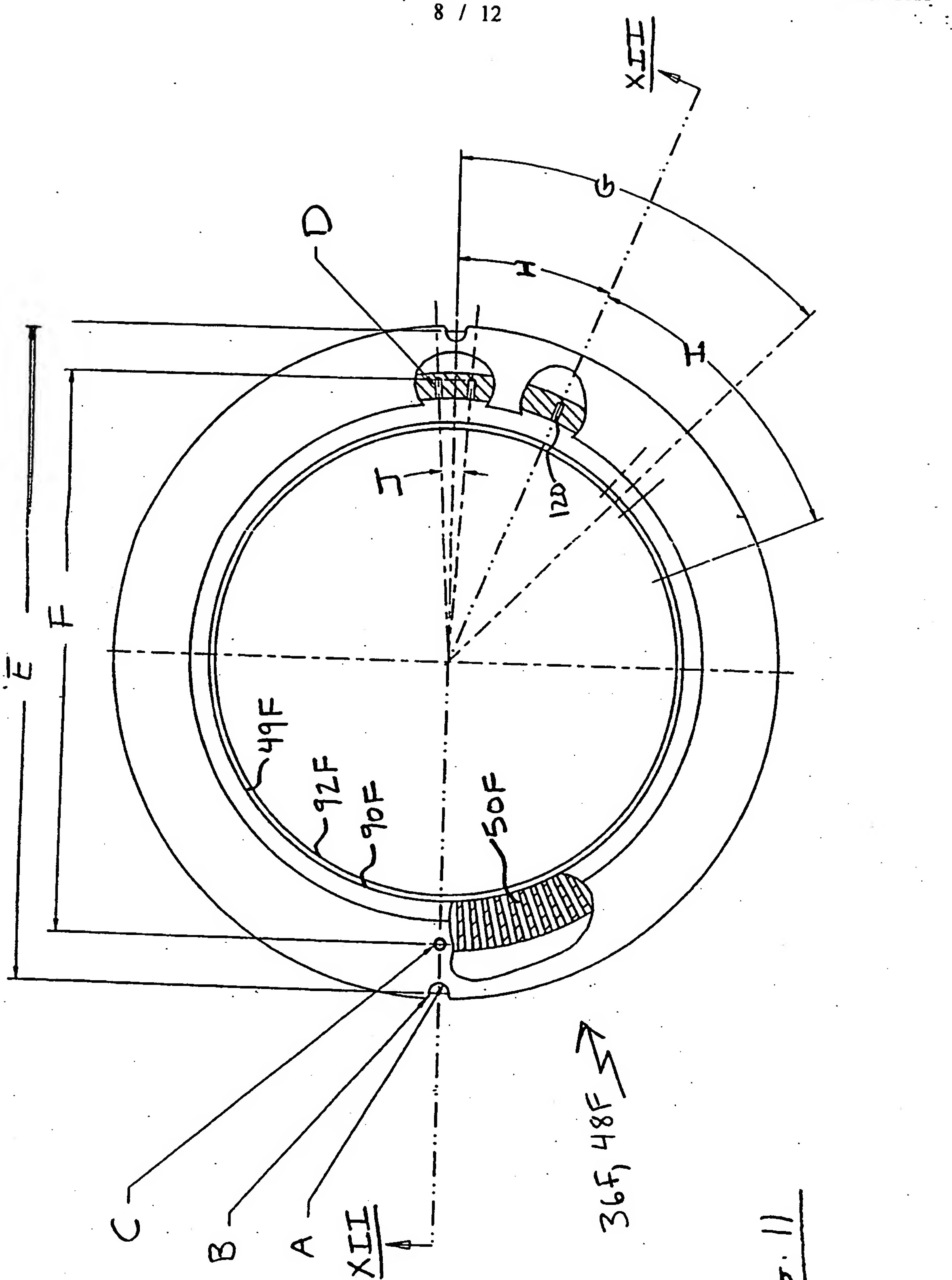


FIG. 11

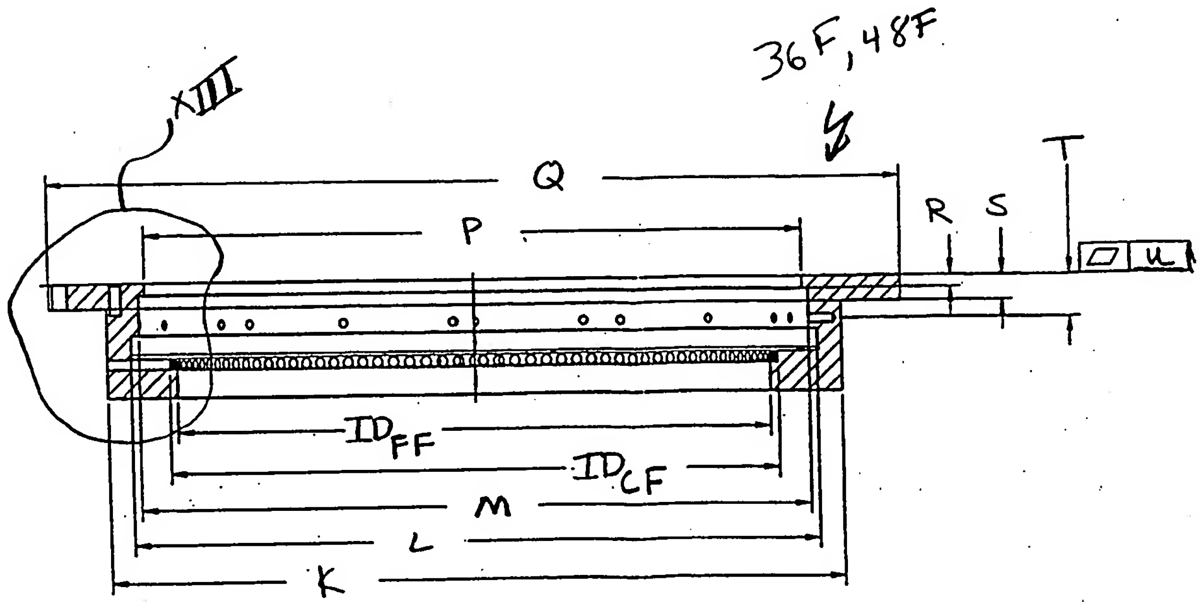

XIII
36F, 48F
Q
P
R
S
T
U
ID_{FF}
ID_{CF}
M
L
K

FIG. 12

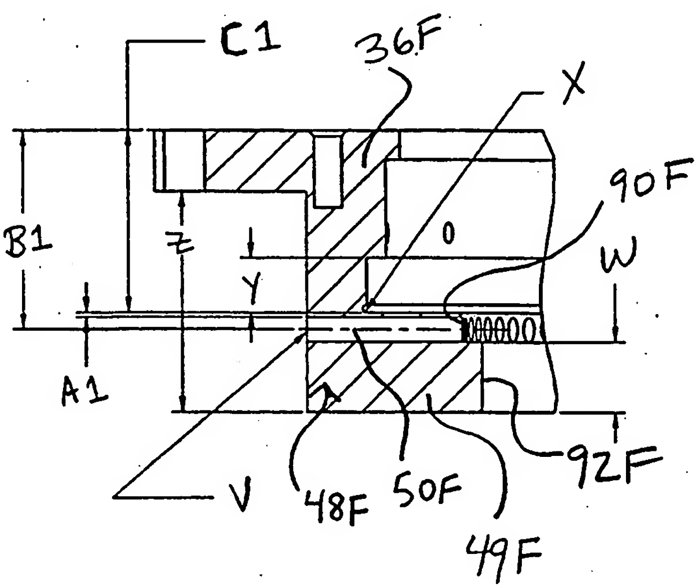

C1
36F
X
90F
B1
Z
Y
W
A1
V
48F
50F
49F
92F

FIG. 13

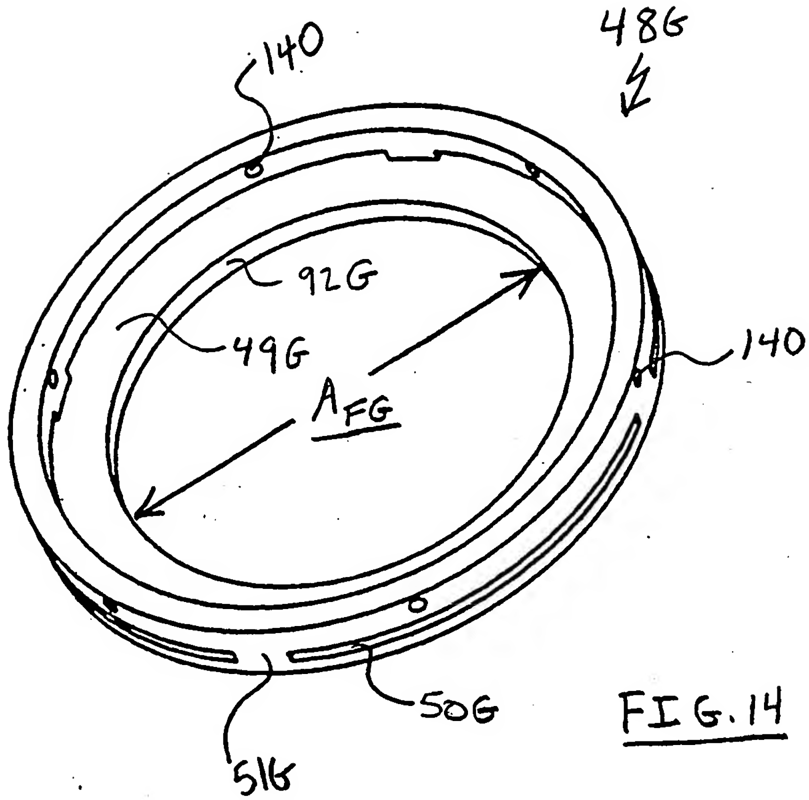


FIG. 14

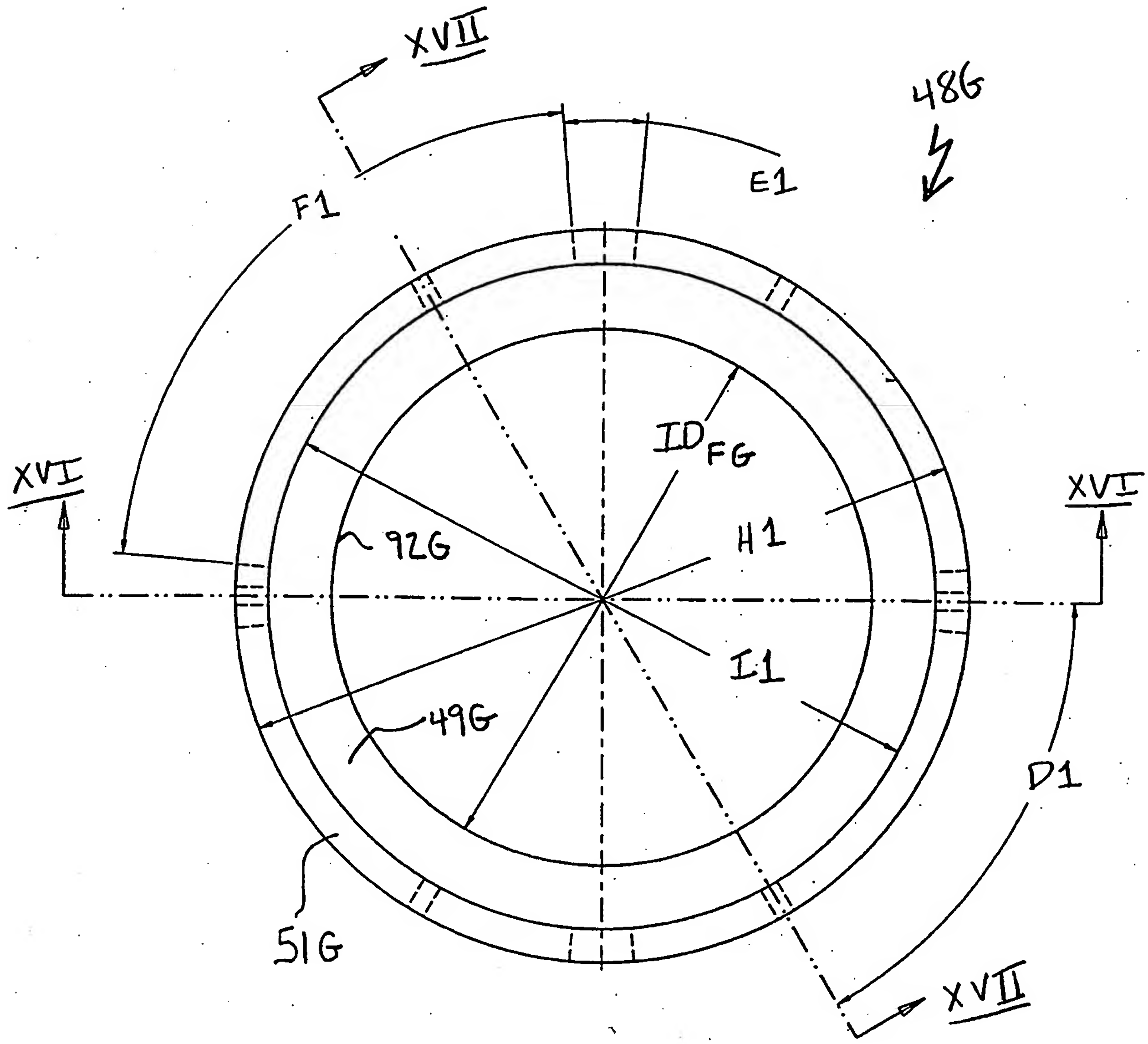


FIG. 15

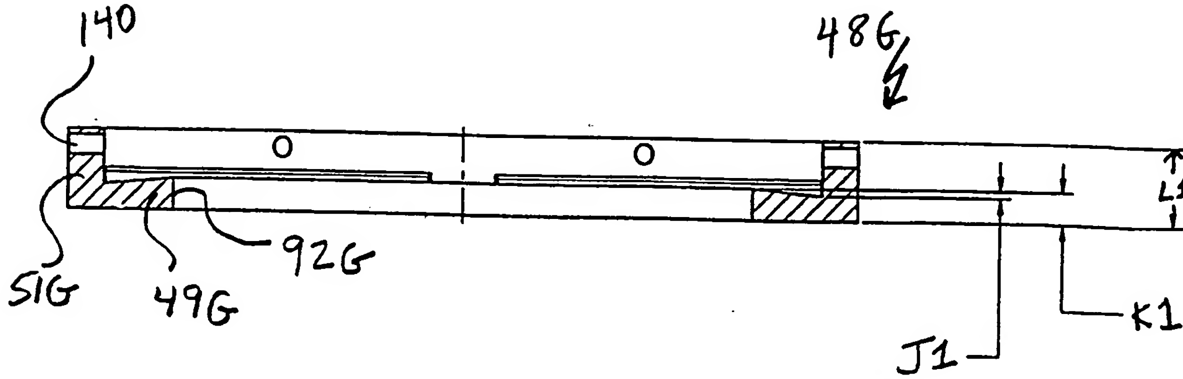


FIG. 16

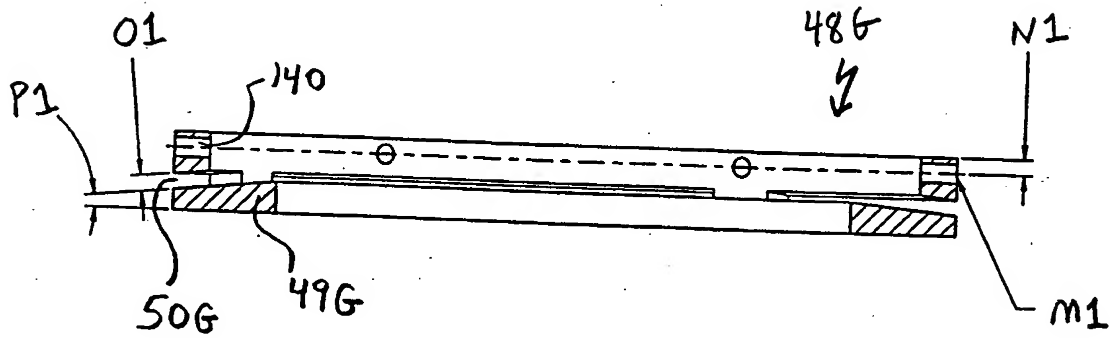


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/22825

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : C25D 5/02, 5/04, 7/12, 17/00, 17/08
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 204/ 212, 224R, 237, 279, 297R, Dig. 007; 205/95, 96, 118, 133, 137, 143, 151, 157, 291

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
Search terms: flange, annulus, 205/clas

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,246,088 A (MURPHY ET AL) 20 January 1981,col. 3, lines 57-58; col. 4, lines 27-35.	1, 7
Y	US 4,259,166 A (WHITEHURST) 31 March 1981, col. 2, lines 12-60, col. 3, lines 1-35, col. 4, lines 1-27.	1, 5-7, 11-12, 15, 17-21, 23-26, 30-32
Y	US 4,466,864 A (BACON ET AL) 21 August 1984, Figures and col. 4, lines 4-32,	1, 15-17, 19-21, 23-27, 31
Y	US 5,441,629 A (KOSAKI) 15 August 1995, col. 6, lines 10-40	23-25, 27, 31
A	US 5,135,636 A (YEE ET AL) 04 August 1992, col. 5, lines 1-30.	23-25

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 FEBRUARY 1999	18 FEB 1999

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/22825

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

204/ 212, 224R, 237, 279, 297R, Dig. 007; 205/95, 96, 118, 133, 137, 143, 151, 157, 291

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